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A New Differential Logic-Compatible Multiple-Time Programmable (MTP) Memory Cell

Yi-Hung Tsai, Hsiao-Lan Yang, Wun-Jie Lin, Chrong Jung Lin, and Ya-Chin King

Microelectronics Laboratory, Semiconductor Technology Application Research (STAR) Group,
Institute of Electronics Engineering, National Tsing-Hua University, Hsin-Chu 300, Taiwan
Phone/Fax: +886-3-5715131-34034/+886-3-5721804, E-mail: cjlin@ee.nthu.edu.tw

1. Introduction

With the growing popularity of nonvolatile storages, the embedded non-volatile memory (NVM) technology, which integrates logic CMOS and NVM within the same chip, has an increasing demand ranging from low-bit applications such as RFID tags to mega-bit code storage. The RFID application requires low cost, and focuses on the reliability of memory cells and the integration with peripheral circuit. Some logic compatible NVM solutions have been proposed to deduce the fabrication cost [1-3]. The limited scaling of gate oxide thickness in floating gate device obstacles the integration of embedded NVM in advanced technology. However, the data retention issue has been effectively retarded by differential memory structure [4].

In this paper, we propose a novel differential n-channel Multiple-Time Programmable (MTP) memory for the fully compatible logic NVM applications. In addition, a self-selective program technique is innovated to write and read a pair differential data in one cell instead of the complicated and size-consuming overhead circuit for achieving same kind of purpose [3, 4]. The superior on/off window of the cell is also performed in retention and endurance to challenge thin floating gate oxide below 70Å for 90nm CMOS node and beyond.

2. New Cell Structure and Operation Concept

The 3D structure cross-sectional view is shown in Fig. 1(a). The differential cell consists of two identical floating gate (FG) transistors with common p-well, common select gate (SG), and common erase gate (EG). Each differential cell stores one bit, and can be easily arranged into a NOR-type array as shown in Fig. 1(b). The programming scheme of differential operation is shown in Fig. 2. To maximize the window, the logic "1" state is defined as (FG1, FG2)=($V_{TH,high}$, $V_{TH,low}$), while the logic "0" state is defined as (FG1, FG2)=($V_{TH,low}$, $V_{TH,high}$). While programming the cell, page erase is first performed to set all floating gates to $V_{TH,low}$. All floating gates are erased to slight depletion state at zero or minor negative threshold voltage. Moreover, the program sequence includes two sequential steps: the first step uses channel hot electron to program the cell at BL1, so called logic "1" bit. The second step is then a self-selective program to write BL2 data for the bits on the same bitlines. Since the second step is a self-selective program mechanism, we can perform it for the whole chip or sectors at once and no decoding is needed. The novel self-selective program method on logic "0" and logic "1" is illustrated in Fig. 3(a) and 3(b), respectively. It describes the programming path from BL2 to BL1 during the self-selective program. In the case of logic "0" programmed as shown in Fig. 3(a), FG1 is just at erase state, that is, at depletion mode, therefore, FG2 can be programmed via the path from BL2 to BL1, and ($V_{TH,low}$, $V_{TH,high}$) is achieved. In addition, considering logic "1" state as shown in Fig. 3(b), since FG1 is already programmed in the first step, the path from BL2 to BL1 is shutoff. The FG2 will not be changed from erase state after the following self-selective operation, resulting in the bit kept at ($V_{TH,high}$, $V_{TH,low}$). Due to the unique self-selective characteristics, the self-selective program can be performed on the whole chip or some sectors at once, the timing of decoders and buffers can be released for next data input or high voltage charging/discharging. The novel MTP cell and its operation successfully reduces and simplifies the complicate work of peripheral circuits in decoding, readout, sensing, and re-write for achieving the differential bit data storage for thin floating gate oxide applications.

3. Results and Discussion

The cells are demonstrated in pure 0.18μm CMOS logic process without any additional mask and process step. The cell has 3.3V I/O gate oxide thickness around 70Å. The program and erase characteristics are exhibited in Fig. 4 and Fig. 5. According to the characterization, the MTP cell can be programmed within 1ms at VBL=7V, and erased within 30ms at VFN=9.5V. Moreover, the characterization of self-selective program is shown in Fig. 3. The step of self-selective program can be finished within 300ms and no disturb occurs in logic "1" bit. The operation conditions are summarized in Table 1. Fig. 6 shows the read disturb and it clearly reveals there is no disturb concern after 10 years continuous DC stress at VBL=1.8V. The program disturb is also characterized and the superior disturb window is shown in Fig. 7. Figure 8 shows the data retention characteristics, there is no significant degradation after 1000hr baking at 85^{o}C and 125^{o}C. Figure 9 shows the 100K cycles of endurance results. There is only little degradation in on-state due to several electron traps in gate oxide after long term program/erase operations.

4. Conclusion

A new differential MTP memory cell and operation have been proposed and demonstrated in the paper. The innovative cell features double sensing window, good program and erase speed, and excellent reliability. The new differential cell and its novel operation method will be a very promising MTP solution for the gate oxide below 70Å in advanced CMOS logic NVM applications.

References

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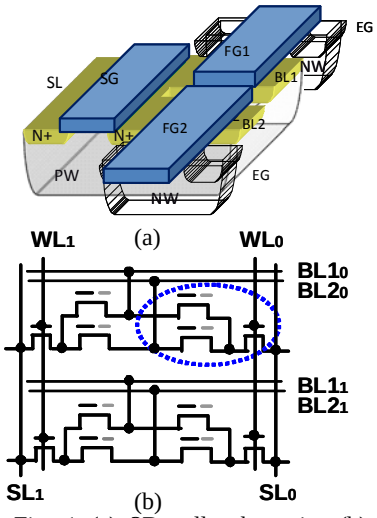

Fig. 1 (a) 3D cell schematics (b) NOR-type array arrangement. The gray line of each transistor denotes the erase gate. Common erase gate connection is not plotted here for simplicity.

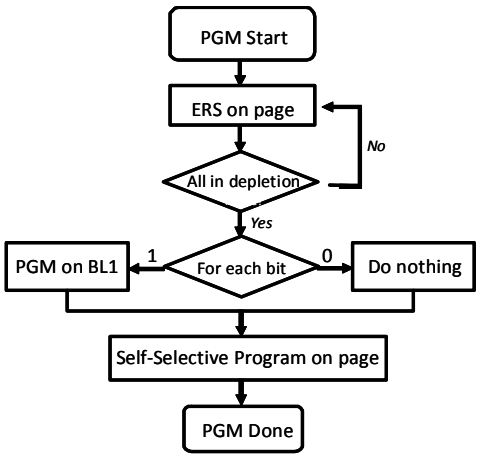

Fig. 2 The new two-step programming scheme.

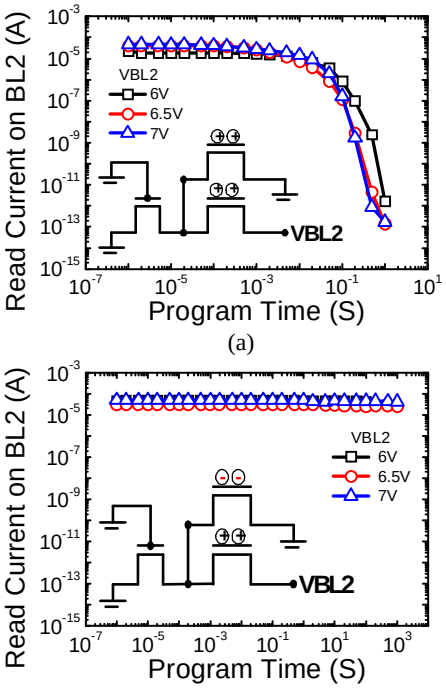

Fig. 3 Self-selective programming on (a) (FG1,FG2)=($V_{TH,low}$, $V_{TH,low}$) (b) (FG1,FG2) = ($V_{TH,high}$, $V_{TH,low}$). After the second step programming, (a) becomes ($V_{TH,low}$, $V_{TH,high}$) and (b) remains ($V_{TH,high}$, $V_{TH,low}$). The two-step program is then finished.

Table 1 Cell Operation

	BL1		BL2		WL		EG	SL
	Select	Unselect	Select	Unselect	Select	Unselect		
Program	7V	0V	floating	floating	3.3V	0V	floating	0V
Self-Selective Program	0V		7V		0V		floating	0V
Erase	0V		0V		0V		9.5V	0V
Read	1V	0V	1V	0V	2V	0V	floating	0V

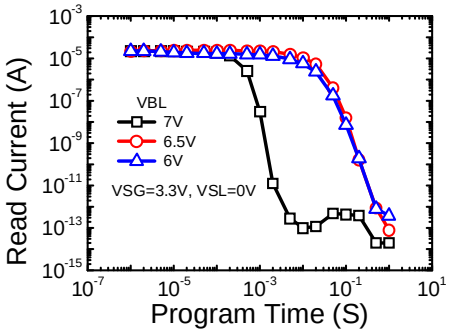

Fig. 4 Program characteristics by channel hot electron injection.

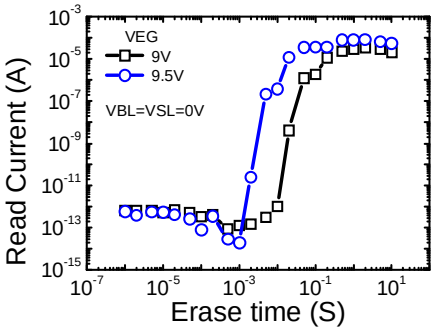

Fig. 5 Erase characteristics at FN operation.

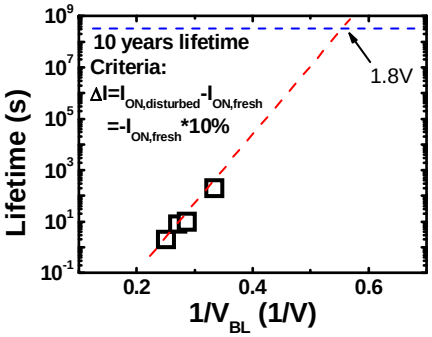

Fig. 6 Read disturb and the lifetime prediction. The cell can sustain continuous VBL=1.8V DC stress for 10 years

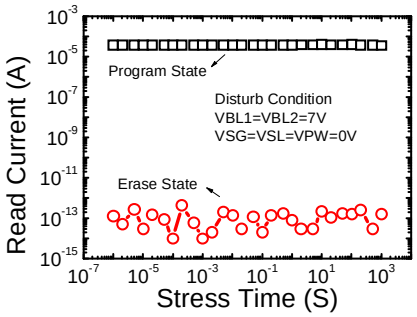

Fig. 7 Drain Disturb on unselected WL. The unselected cell show excellent immunity to high drain voltage over 1000s

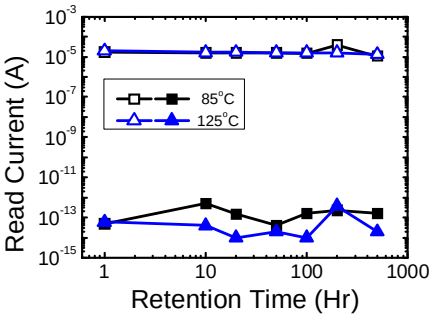

Fig. 8 Data retention characteristics at 85°C and 125°C. No significant charge loss after 1000hr baking at 125°C

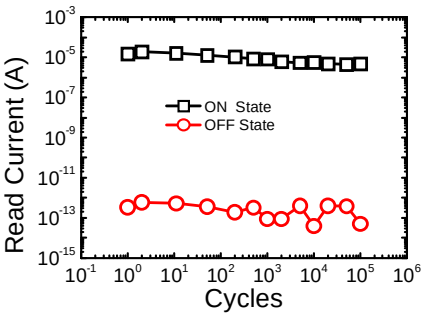

Fig. 9 On-state current is slightly degraded post 100k cycling.