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Overview and Future Challenges of High Density FeRAM

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1. Introduction

A high density FeRAM (Ferroelectric Random Access Memory) has been a promising candidate for a universal memory due to its nonvolatile, low power consumption, high endurance and high-speed read/write characteristics for more than 20 years. Some fundamental researches show excellent thickness and lateral scalabilities of the ferroelectricity of $PbZr_xTi_{1-x}O_3$ (PZT)[1], $BaTiO_3$ [2] and $PbNb_xZr_yTi_zO_3$ [3], indicating a high potential of the ferroelectric materials for Gb class nonvolatile memories. In spite of these capabilities, today's FeRAM products have started their real applications from relatively low memory densities below 4Mb, targeting IC cards, tags or specific stand-alone memories. Although they are indeed important applications best suited to FeRAMs from the performance requirements and their market demands continue growing rapidly, there are still wide range of applications awaiting higher density FeRAMs.

One of the reasons of such moderation of FeRAM density is the difficulty of ferroelectric capacitor integration into a LSI structure without inducing a polarization degradation using standard CMOS process technologies. If such a difficulty is overcome, excellent circuit technologies exert the best performance of the ferroelectric capacitors, thus realizing a new generation of high density FeRAM that surpasses the other existing nonvolatile memories.

In this paper, the latest status of a high density chain FeRAM™[4] development and some key features of process technologies that realize a highly reliable world's highest density and highest speed 128Mb chain FeRAM[5,6] are presented. Some promising applications for the high density chain FeRAM are also discussed in the presentation.

2. Key Features of 128Mb chain FeRAM Technologies

Table 1 shows device features of the 128Mb chain FeRAM. 130nm standard CMOS technologies with 4-metal layers are used for the integration. A ferroelectric capacitor is made of the stacked layer of Ir/MOCVD-PZT/ $SrRuO_3$(SRO)/IrO_2[7]. A capacitor area is 0.084 um^2, that is less than half of the previous 64Mb generation. The most important technological challenge to shrink the capacitor is to suppress the capacitor degradation during the back end of line (BEOL) integration. Ferroelectric materials with a perovskite structure such as PZT are ionic crystals with weak ionic bonds between oxygen and other constituent metal elements. Due to this ionic nature of the PZT, hydrogen radicals generated during the CMOS integration processes such as a plasma passivation film deposition, a reactive ion etching of PZT stack and subsequent contact hole openings reduce the PZT especially at a ferroelectric /electrode interface and degrade the polarization reversal of the capacitor. Although such a general understanding comes mostly from the researches of oxygen vacancy behavior in bulk ceramics perovskite oxides[8], it is surprisingly still applicable to the thin ferroelectric films.

	THIS WORK	Previous
Density	128Mb	64M
Bandwidth	1.6GB/s (DDR2)	200MB/s
Architecture	Octal Bit Line	Quad Bit Line
Chip Size (mm^2)	87.7	87.
Cell Size (um^2)	0.25	0.6
Capacitor Size (um^2)	0.084	0.1
Array Voltage (V)	1.5	1.8
Capacitor	IrO_2/SRO/PZT/Ir/TiAlN	⟵
Cell Layout	Half Pitch	Normal Pitch
Capacitor Shape	Triangle	Rectangle
Metallization	4-level Al	3-level Al
Technology Platform	130nm CMOS	⟵

Table 1. Device features of 128Mb chain FeRAM in comparison with previous 64Mb chain FeRAM.

Figure 1 shows an extrapolation of signal voltages of small capacitors fabricated using 64Mb generation technologies. Since a signal voltage of 300mV is required for a reliable 1T1C operation[5], it is evident that a simple application of previous generation technologies for the 128Mb or higher density FeRAMs is not acceptable. Based on the degradation mechanism of the ferroelectric capacitors mentioned above, several sophisticated technologies are introduced to realize the 128Mb chain FeRAM. First, a low-damage capacitor RIE technology is developed. During the capacitor etching, a sidewall of the PZT is exposed to a plasma atmosphere and bombarded by high-energy particles. This process step induces oxygen deficiency on the PZT sidewall and forms a 'dead layer' around the periphery of the capacitor stack. Such an effect evidently becomes severer for smaller capacitors. One logical approach to reduce this degradation is to suppress the chemical reaction of PZT with etching chemistries by lowering an RIE temperature. Figure 2 shows the impact of the RIE temperature for the small capacitors. At below 300C the capacitor degradation is effectively suppressed and more than 60% higher signal value is obtained than the

case at 350C. However, since the lower RIE temperature causes a lager sidewall taper angle of the capacitor requiring a larger footprint of a memory cell, a careful control of the RIE conditions other than the temperature is required.

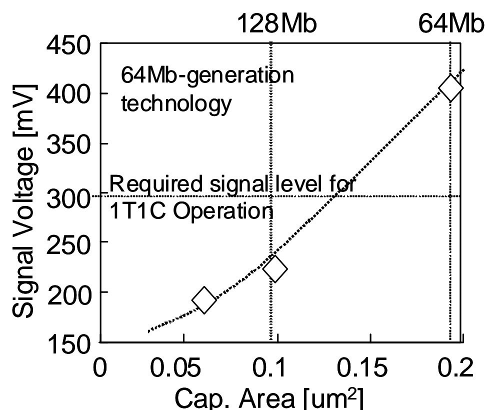

Fig. 1. Estimated signal voltage of 128Mb generation capacitor fabricated using 64Mb generation technology

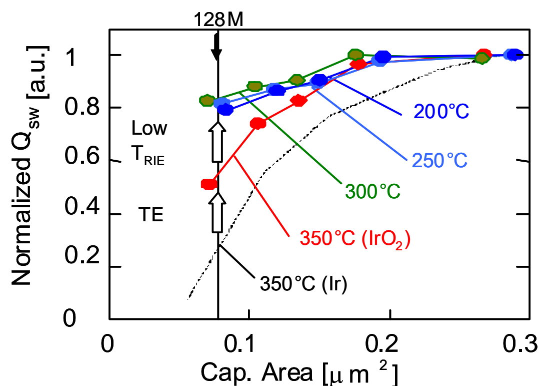

Fig. 2. Normalized switching charge (Qsw) at each RIE temperature as a function of capacitor area.

Second, a more straight forward approach is to increase the capacitor area most effectively in a limited cell area. For this purpose, an area effective triangular capacitor with a half-pitch layout is introduced. Figures 3 (a) and (b) show a plan view and a bird-eye view SEM photographs of the newly designed triangular capacitors, respectively. This structure increases the area efficiency by 17% compared to the rectangular capacitor with a normal-pitch layout adopted in the previous generation.

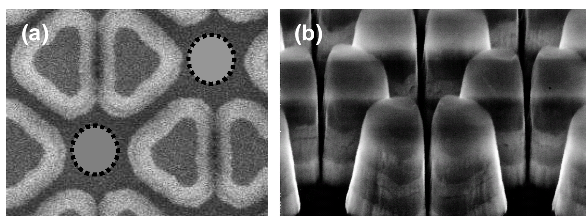

Fig. 3. A plan view (a) and a birds-eye view (b) SEM photographs of area effective triangular capacitors in half-pitch layout.

With a combination of the other key technologies such as a high-density hydrogen diffusion barrier layer as well as innovative circuit designs such as an octal bit-line architecture[6], the signal voltage criteria of more than 300mV is sufficiently satisfied as shown in Fig. 4.

It should also be noted that the chain FeRAM has the potential to realize a high bandwidth due to its fast access and low read/write energy per bit characteristics. A 400MHz DDR2 interface installed in the 128Mb chain FeRAM achieves the highest 1.6GB/s read/write bandwidth in nonvolatile memories reported so far as indicated in Fig. 5. This high speed performance can create a foothold in such new FeRAM applications as currently covered by DRAMs.

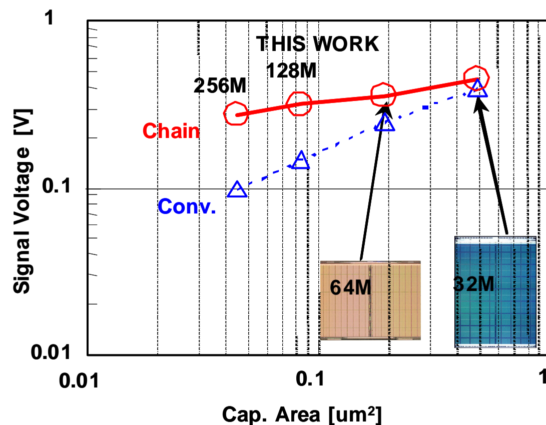

Fig. 4. Signal voltage in each generation as a function of capacitor area with improved technologies.

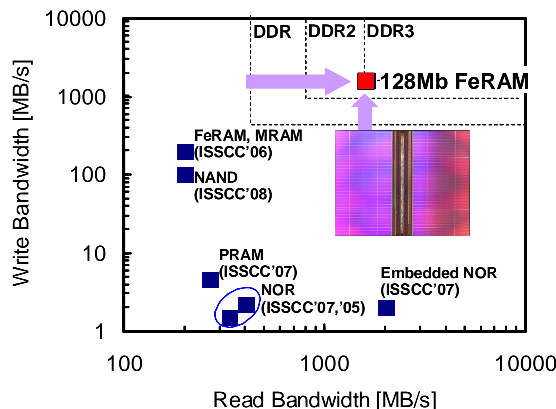

Fig. 5. Trend of read/write bandwidth for various nonvolatile memories.

3. Summary

In summary, the latest status of a high density FeRAM development has been presented based on the world's highest density and highest speed 128Mb chain FeRAM. Some key process and design technologies have been provided and demonstrated a novel performance that opens a door to wider FeRAM applications.

References

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