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A Negative Word-line Voltage Step-Down Erase Pulse Scheme with $\Delta V_{TH}=\frac{1}{6}\Delta V_{ERASE}$ for Enterprise SSD Application Ferroelectric(Fe)-NAND Flash Memories

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1. Introduction

An enterprise SSD for data centers are paid much attention as a future market of flash memories [1,2]. For an enterprise SSD, a Ferroelectric(Fe)-NAND flash memory is suitable because it decreases the program/erase voltage from 20V of the floating-gate (FG)-NAND to 6V and the write/erase cycles increases from 10^4 to 10^8 cycles [3]. The Fe-NAND consists of a series connected MFIS, Metal Ferroelectric Insulator Semiconductor transistors (Fig.1). By applying a program/erase voltage, the electric polarization in the ferroelectric layer flips and the memory cell V_{TH} shifts (Fig.2). An Hf-Al-O buffer layer between a ferroelectric layer and a Si substrate realizes a 10-year data retention [3]. A non-volatile page buffer achieves a power outage immune highly reliable operation [4]. In the NAND cell array, the memory cell V_{TH} must be lower than the read voltage. In the FG-NAND, as the program V_{TH} is higher than the erase V_{TH}, a narrow program V_{TH} distribution is realized with a bit-by-bit verify program [5]. In the Fe-NAND, as the erase V_{TH} is higher than the program V_{TH}, a narrow erase V_{TH} distribution is required with a bit-by-bit verify erase (Fig.3). To realize a bit-by-bit verify erase and control the erase V_{TH} precisely, this paper proposes a negative word-line voltage step-down erase pulse scheme. The proposed scheme realizes two key requirements, 1) a short rising time of erase pulses and 2) a constant V_{TH} shift, ΔV_{TH}, for each erase pulse.

2. Negative Word-line Voltage Erase

In the conventional well erase (Fig.4(a)), charging a huge well capacitance, 10nF takes as much as 1ms. As the bit-by-bit verify requires 5-10 pulses, the erase time is 20ms per page and over 2sec per block, which is one thousand times longer than the program/erase time of the FG-NAND. In the proposed negative word-line voltage erase (Fig.4(b)), the load is a word-line with 2-3pF. As the rising time is 2us, the erase pulse width is shortened to 10us that is the same as the program pulse width of the FG-NAND. As a result, a 200us/page fast erase is realized.

3. Step-Down Erase Pulse

Next, a step-down erase pulse (Fig.5(c)) is proposed to realize a constant ΔV_{TH}. The erase voltage, V_{ERASE} starts with $V_{INITIAL}$ and decreases by ΔV_{ERASE}. This paper experimentally demonstrates for the first time that in the Fe-NAND, ΔV_{TH} is constant with a step-down erase pulse (Fig.6). In contrast, the fixed pulse (Fig.5(a)) and the variable time pulse (Fig.5(b)) show over 200% ΔV_{TH} variation. Fig.7 and 8 show the measured ΔV_{TH} for ΔV_{ERASE} of 0.4V and 0.1V, respectively. If $V_{INITIAL}$ is small e.g. -2V, ΔV_{TH} for the 1st pulse is small (0.01V). If $V_{INITIAL}$ is large e.g. -4V, ΔV_{TH} is also large, 0.27V. Yet, at erase time of 100us, the measured ΔV_{TH} converges to 0.07V and 0.016V for ΔV_{ERASE} of 0.4V and 0.1V regardless of $V_{INITIAL}$. Thus, the proposed scheme is robust against the $V_{INITIAL}$ variation. When the V_{TH} reaches the target voltage by using the proposed step-down erase pulse, ΔV_{TH} becomes constant and a precise erase V_{TH} control is realized. Based on the measured ΔV_{TH} as a function of ΔV_{ERASE} (Fig.9), this paper reports for the first time an important formula, $\Delta V_{TH}=1/6\Delta V_{ERASE}$, for the Fe-NAND that is completely different from the formula, $\Delta V_{TH}=\Delta V_{ERASE}$, for the FG-NAND (Table I)[6].

In an actual erase operation, all memory cells connected to the same word-line are erased at the same time. The variation of device parameters such as the ferroelectric layer thickness causes an erase speed variation. Fig.10 shows the erase characteristics of the fastest and the slowest cells. When the fastest cell is successfully erased at the 1st pulse, the V_{TH} of the slowest cell is ΔV_{TH0} lower than the verify voltage. Since the V_{TH} shifts by $1/6\Delta V_{ERASE}$ at each pulse, the slowest cell reaches the verify voltage after $6\Delta V_{TH0}/\Delta V_{ERASE}$ cycles. As a result, the erase V_{TH} distribution becomes $1/6\Delta V_{ERASE}$. By selecting ΔV_{ERASE} at 0.4V, the erase V_{TH} distribution width becomes 0.07V. Fig.11 and 12 show measured erase characteristics and measured ΔV_{TH} for cells with the V_{TH} ranging from -0.3V to 0.05V. Again, ΔV_{TH} is constant at $1/6\Delta V_{ERASE}$ and immune to the V_{TH} variation.

4. Discussion

The mechanism of the constant ΔV_{TH} is explained with the polarization-electric field curve (Fig.13). States "A", "B",…"E" are in minor loops. When the lowest erase voltage, $V_{INITIAL}$, is applied to the memory cell, the memory cell is "A". During the 1st verify, the memory cell moves to "B". At the 2nd erase pulse, the memory cell moves to a larger hysteresis loop and becomes "C". At the 2nd verify, the memory cell is "D". Compared with "B", the polarization at "D" is larger and the V_{TH} becomes higher. At the 3rd erase pulse, the memory cell moves to a larger loop and becomes "E". At the 3rd verify, the memory cell is "F" and the V_{TH} becomes higher than that of "D". By increasing V_{ERASE}, the memory cell transfers to a larger loop and thus the V_{TH} increases until it reaches to the saturation loop [7].

5. Conclusions

A negative word-line voltage step-down erase pulse scheme is proposed for Ferroelectric(Fe)-NAND flash memories. The negative word-line voltage erase accelerates the erase pulse ramp-up from 1ms of the conventional well erase to 2us and a 200us/page erase is realized. With the step-down erase pulse, the erase voltage, V_{ERASE} decreases by ΔV_{ERASE}. The measured V_{TH} shift, ΔV_{TH}, is constant at $1/6\Delta V_{ERASE}$, which is different from that of the floating-gate NAND where $\Delta V_{TH}=\Delta V_{ERASE}$. By combining the proposed scheme with the bit-by-bit verify, a 0.07V erase V_{TH} distribution is achieved with ΔV_{ERASE} of 0.4V.

Acknowledgements

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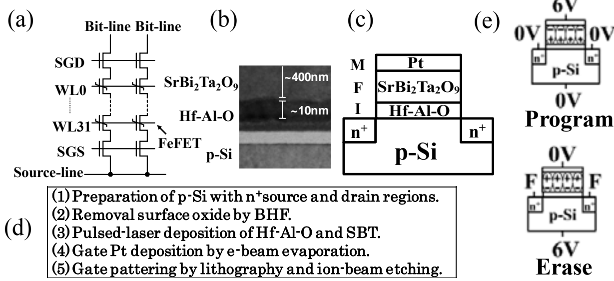
References

[1] K. Takeuchi, *ISSCC*, Tutorial T7 (2008).
[2] K. Takeuchi, *Symp. VLSI Circuits, pp.124-125 (2008).*
[3] S. Sakai et al., *NVSMW, pp.124-125 (2008).*
[4] T. Hatanaka et al., *Symp. VLSI Circuits (2009).*
[5] T. Tanaka et al., *Symp. VLSI Circuits, pp.168-169 (1996).*
[6] G. J. Hemink et al., *Symp. VLSI Technology, pp.129-130 (1995).*
[7] B. Jiang et al., *Symp. VLSI Technology, pp.141-142 (1997).*



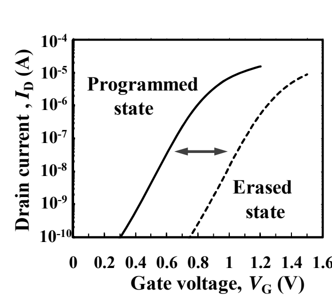


Fig. 1 (a) Fe(Ferroelectric)-NAND flash memory cells [3]. (b) SEM photograph. (c) Fe-NAND cell structure. (d) Process flow. (e) Program and erase bias condition.

Fig. 2 I_D-V_G characteristics after the program and the erase [3].

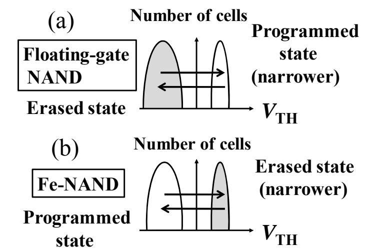


Fig. 3 V_{TH} distribution of
(a) Floating-gate NAND cell and
(b) Fe-NAND cell.

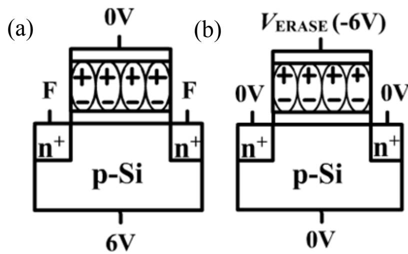


Fig. 4 (a) Conventional erase scheme.
(b) Proposed negative word-line voltage erase scheme.

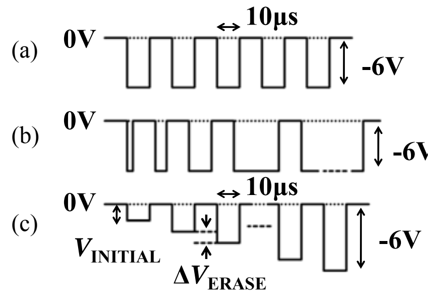


Fig. 5 (a) Fixed erase pulse.
(b) Variable time erase pulse.
(c) Proposed step-down erase pulse.

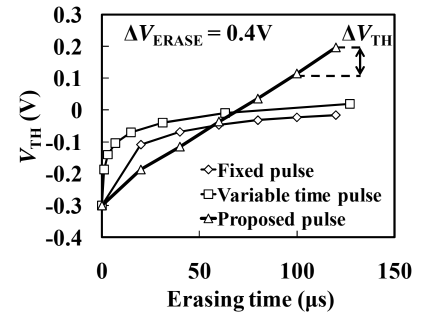


Fig. 6 Measured erase characteristics. Erase pulse width / $V_{INITIAL}$ of the proposed scheme are 10us/ -3V.

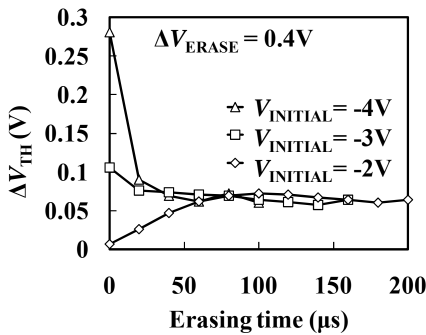


Fig. 7 Measured ΔV_{TH} with ΔV_{ERASE} = 0.4V. Erase pulse width is 10us.

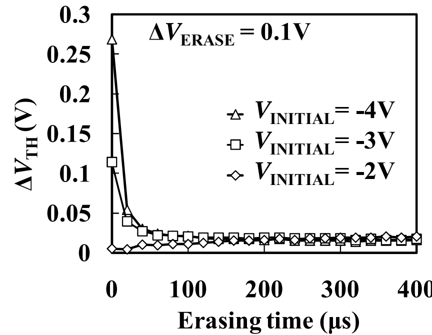


Fig. 8 Measured ΔV_{TH} with ΔV_{ERASE} = 0.1V. Erase pulse width is 10us.

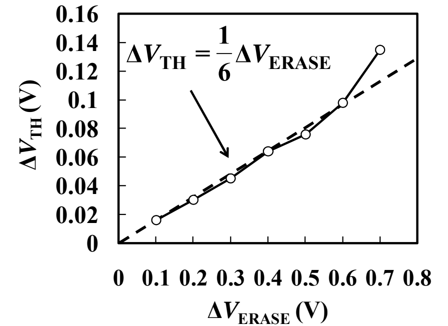


Fig. 9 Measured V_{TH} shift, ΔV_{TH} as a function of ΔV_{ERASE}. Erase pulse width is 10us. $V_{INITIAL}$ = -3V.

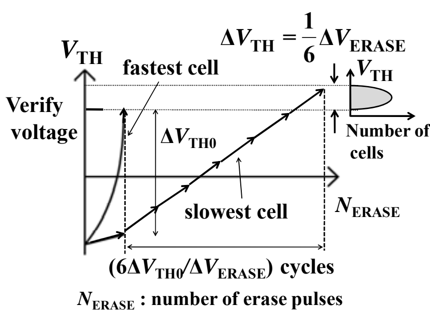


Fig. 10 Erase characteristics of the fastest and the slowest cells.

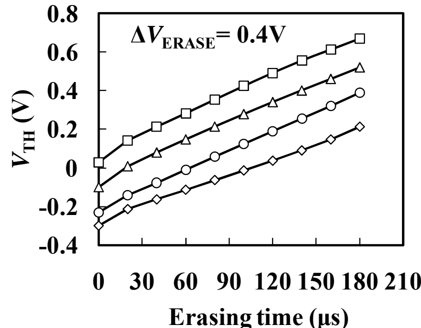


Fig. 11 Measured erase characteristics for cells with various V_{TH}. Erase pulse width is 10us. $V_{INITIAL}$ = -3V.

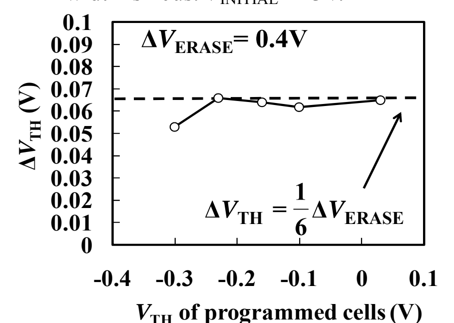
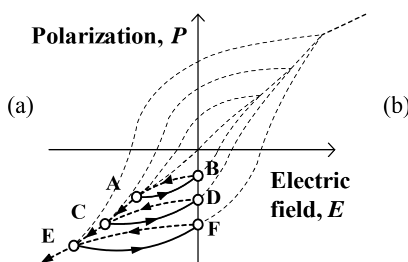


Fig. 12 Measured ΔV_{TH} for cells with various V_{TH}. Erase pulse width is 10us. $V_{INITIAL}$ = -3V.



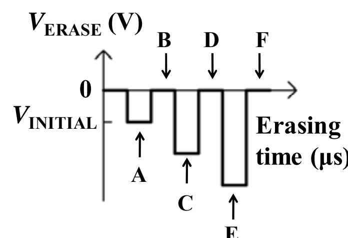


Fig. 13 Model of the constant V_{TH} shift, ΔV_{TH}, for the step-down erase pulse scheme.

Table I Relationship between ΔV_{TH} and ΔV_{ERASE}.

Floating-Gate NAND Cell	Fe-NAND Cell
$\Delta V_{TH} = \Delta V_{ERASE}$	$\Delta V_{TH} = \frac{1}{6}\Delta V_{ERASE}$