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High-Speed Multilevel Resistive RAM Using RTO WO_X

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1. Introduction

Resistance-based memory has attracted much attention because of its small cell size, simple structure, high speed, and high thermal stability [1-3]. WO_X based RRAM requires only one extra non-critical mask, no new equipment or new material from the standard CMOS process and is thus especially attractive [4]. Although plasma oxidation produced WO_X with reasonable performance, however, the resistance window is relatively small so the MLC capability is limited [5]. In this work we report for the first time the WO_X RRAM using rapid thermal oxidation (RTO). Through this new RTO oxidation process, we gain a 10X resistance window, which is more suitable for MLC operation. Both 2-bit/cell and 3-bit/cell operations are examined. Further, low-voltage and high-speed operations are also investigated.

2. Device Fabrication

Figure 1 shows the cross sectional TEM image and the process flow of the RTO WO_X resistive memory. The fabrication process flow follows the conventional back-end-of-line W-plug process. The RTO is performed at 500^{o}C in oxygen ambient. The thickness of WO_X film is about 660Å. The WO_X active area is located between the W bottom electrode (BE) and the TiN top electrode (TE).

3. Results and Discussions

Figures 2 and 3 show the intrinsic pulse R-V characteristics by positive and negative pulses. Positive pulses reset the device to high resistance states, and negative pulses set the device to a low resistance state. However, the required pulse amplitudes are relatively high. Similar to the WO_X fabricated by plasma oxidation [4], after applying a forming step (3.5V/50ns) to the cells, the programming voltages are dramatically reduced (Fig. 4), and the cells are stable for normal operations. The cell resistance is then checked after different 50ns programming pulses. The resistance increases from the low resistance state (LRS) to the high resistance state (HRS) as the pulse amplitude increases. The resistance window of our RTO WO_X is 10X of the plasma-oxidized sample [1]; this indicates the performance of WO_X RRAM is strongly dependent on the oxidation process. Figure 5 shows the R-V curves from cells with different contact sizes after forming. With a smaller contact, the cell shows a lager resistance window, which is beneficial for scaling. Figure 6 shows programming voltages required for successful SET and RESET operations for 50 cells. The tight distributions mean the contact size and the RTO WO_X are both uniform. More interesting is that the RTO WO_X device presents excellent cycling endurance—a resistance window (from 10KΩ to 50KΩ) is maintained very well even after 10^8 cycles (1.4V, 50ns for RESET and -1.2V, 50ns for SET), as shown in figure 7. For high speed testing, the pulse IV characteristics of the RTO sample are collected through a customized high-speed tester [6]. The transient I-V characteristics for both RESET and SET operations are shown in figures 8 and 9. The RESET pulse width is only 2ns, and the equivalent current density is about $3.4x10^6$A/cm^2. Successful SET is achieved by a 2ns pulse with an equivalent current density of $3.3x10^6$A/cm^2. The transient currents for RESET and SET operations with different pulse widths ranging from 2ns to 100ns are shown in Fig. 10. Both SET and RESET currents show slight pulse width dependence. Short pulse width can reduce the SET and RESET currents. Figure 11 shows the cell resistance after programming pulses with different pulse widths. Compared to Fig. 10, the RESET resistance remains at the same level but the SET resistance decreases as the pulse width increases.

Excellent 2-bit/cell operation to more than 10^4 cycles is shown in Fig. 12. A 10KΩ resistance window is maintained for all adjacent states. The state 00, which is the LRS, is achieved by a –1.2V, 50ns SET pulse. The HRS 01, 10, and 11 are obtained by applying 50ns of 1V, 1.2V, and 1.4V pulses, respectively. Figure 13 shows good immunity to read disturb for all states up to 0.5V. Figure 14 illustrates a 3-bit/cell operation RTO WO_X RRAM using a carefully designed P-V (program-verify) algorithm. The resistance window is more than 3KΩ for all adjacent states while cycling endurance is more than 8,000 times.

4. Summary

Excellent cycling endurance (up to 10^8 times) and low voltage (1.4V) operation are demonstrated by RTO WO_X RRAM. The new device exhibits a 10X larger resistance window than plasma oxidized device and provides a better base for MLC operation. The switching speed is extremely fast (~2ns), and the equivalent programming current density is ~$3x10^6$A/cm^2. Two-bit/cell operation with 10K cycle endurance and 3-bit/cell operation with more than 8K cycle endurance are demonstrated. This RTO WO_X RRAM is promising for high-density memory applications.

References

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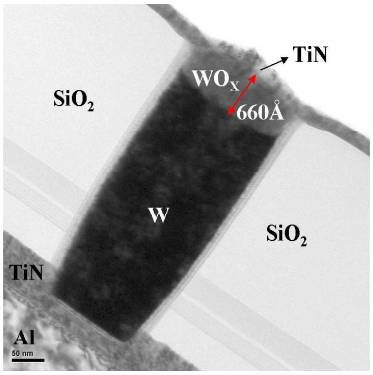

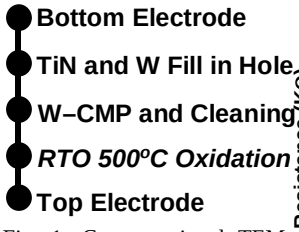

Fig. 1. Cross sectional TEM image and process flow for the 500ºC RTO sample.

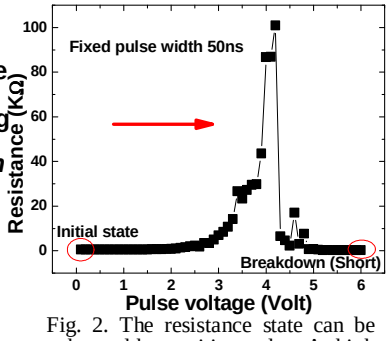

Fig. 2. The resistance state can be enhanced by positive pulse. At high voltage, the device becomes shorted.

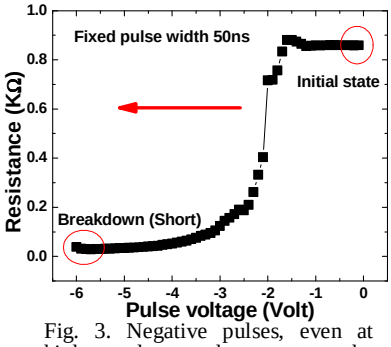

Fig. 3. Negative pulses, even at higher voltages, do not reset the device.

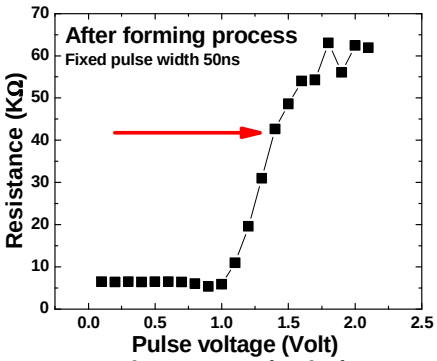

Fig. 4. R-V characteristics after the forming process. Forming process is useful to reduce the switching voltage.

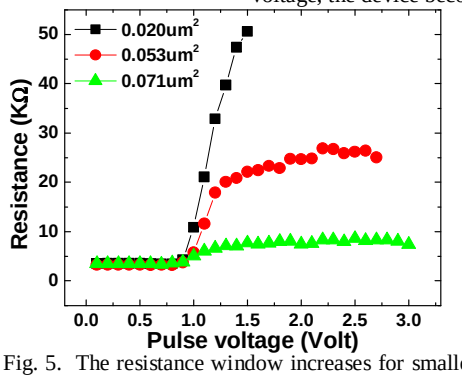

Fig. 5. The resistance window increases for smaller contact area. The devices are treated with a forming process using a 4V/ 50ns pulse first.

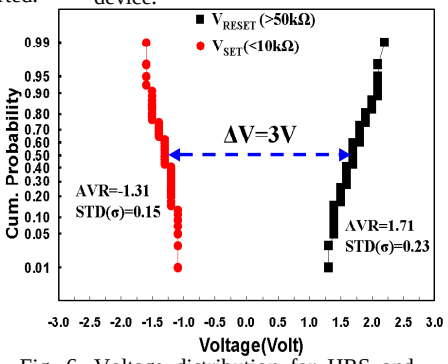

Fig. 6. Voltage distribution for HRS and LRS of 50 memory cells.

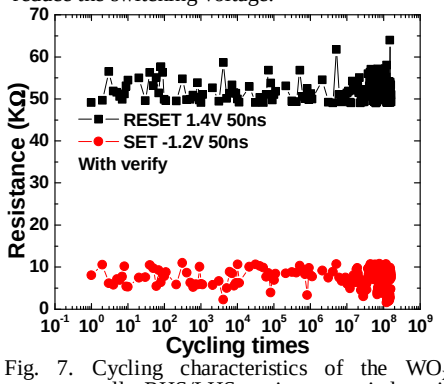

Fig. 7. Cycling characteristics of the WO_X memory cell. RHS/LHS resistance window is well separated at 50k Ω /10k Ω up to > 10^8 cycles.

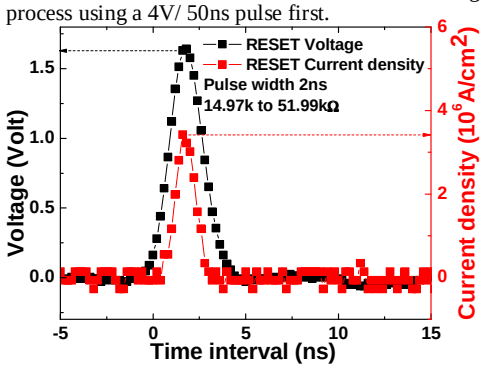

Fig. 8. Time resolved voltage and current traces of RESET operation. The input pulse width is 2ns. The RESET current density is about 3.4x10^6 A/cm^2.

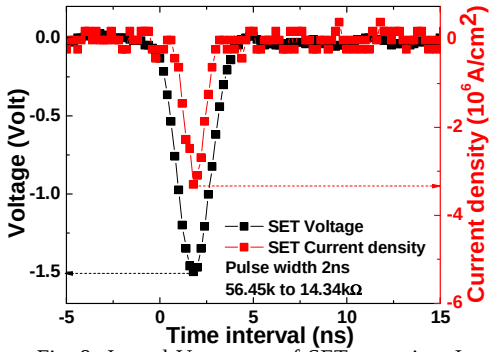

Fig. 9. J-t and V-t curves of SET operation. It also shows high speed erase capability (~2ns). The SET current density is about 3.3x10^6 A/cm^2.

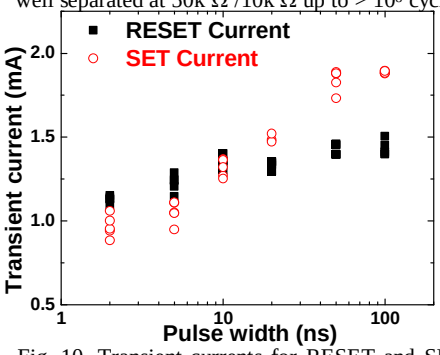

Fig. 10. Transient currents for RESET and SET using various pulse widths.

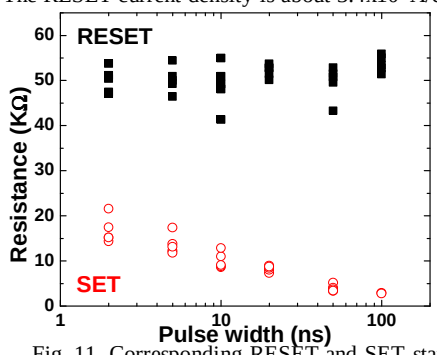

Fig. 11. Corresponding RESET and SET states for various pulse widths.

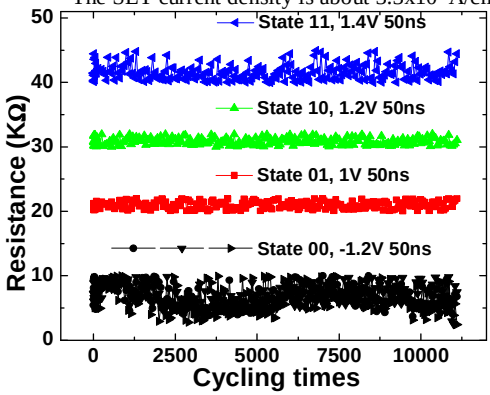

Fig. 12. 4-level cycling test beyond 10^4 cycles with verification. Three RESET states (01,10,11) are programmed by different voltage positive pulses and the SET level (00) is programmed by a negative pulse.

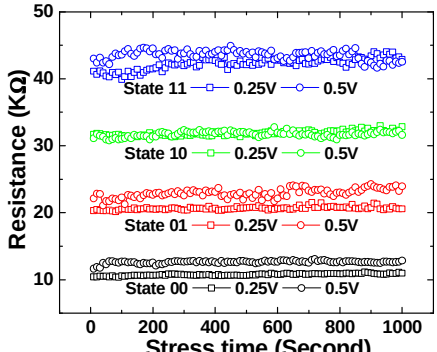

Fig. 13. Read disturb test. All states show acceptable read disturb up to 0.5V.

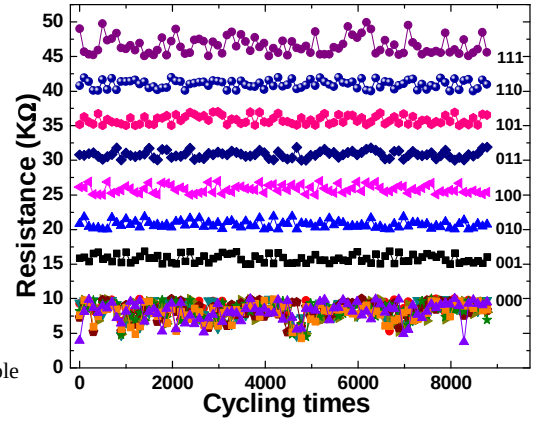

Fig. 14. 8-level cycling test of more than 8k cycles with verification. Well distinguishable resistance windows are maintained for each states.