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MIS Diode Characterization on n-GaN by C-V Measurement at 150℃

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1. Introduction

Compared with AlGaN/GaN heterojunction field effect transistors (HFETs), GaN metal-insulator-semiconductor field effect transistors (MISFETs) have lower leakage current, higher capability of large voltage swings. However, high density of insulator/semiconductor (I/S) interface states greatly undermined the development of GaN MISFETs. Therefore, the characterization about GaN I/S interface traps has been a very important topic[1]. At reverse bias, temperature-dependent transient capacitance measurements of GaN MIS diodes (MISDs) were often used to study the dynamic properties of the GaN I/S interface state charges [2,3]. In these measurements, final stable capacitances (C_{fnl}) have been observed at high temperatures [2, 3]. However, up to now, few researchers have discussed about their origin. In this work, the interface of TEOS-SiO_2/GaN was investigated. We will also discuss whether the C_{fnl} observed in our measurement is related to steady state or thermal equilibrium state, which should be a very important topic for understanding the GaN I/S interface.

By comparing GaN MISDs and Schottky barrier diodes (SBDs) from the same wafer, the relationship between GaN surface potential underneath the SiO_2 (ϕ_{S_MIS}) and gate bias (V_G) was measured for GaN MISDs. Furthermore, by means of thermal- and photo-assistant activation of trapped carriers, the TEOS-SiO_2/GaN interface was investigated by static and transient C-V measurements.

2. Experiments

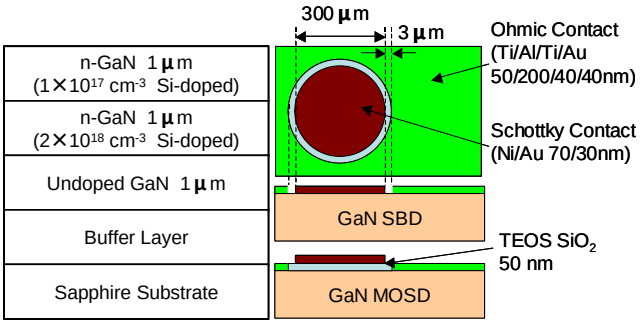


Fig. 1 The epytaxial structure of the wafer (a) and the device patterns for the GaN SBDs and MISDs (b)

n-GaN with Si doping concentration of 1×10^{17}cm^{-3} was used for the MISDs and SBDs, as shown in Fig. 1(a). For the MISDs, 50nm of SiO_2 was deposited on the n-GaN samples at 300℃ by plasma enhanced chemical vapor deposition (PECVD) using 300sccm O_2 and 7sccm liquid source TEOS ($Si(C_2H_5)_4$) with a microwave power of 100W. The pressure for the deposition chamber was controlled at 80Pa. To remove the H and C impurities introduced from the TEOS source[], the as-deposited SiO_2 films were annealed at 1000℃ for 10min in N_2 in a rapid thermal annealing (RTA) system. With magnetron sputtering, Ti/Al/Ti/Au Ohmic contact was formed on the GaN surface where the deposited SiO_2 had been removed using buffered hydrofluoric acid (BHF). Ohmic annealing was performed at 550℃ for 10min in N_2 in the RTA system. Then circular Ni/Au gate contacts with a diameter of 300 μm were deposited on the SiO_2 films with magnetron sputtering. All the SBDs samples were processed at the same time with the MISDs samples except for the SiO_2 related processes. The device pattern was shown in Fig. 1(b).

All the C-V measurements were performed by Agilent 4284A LCR-meter. The measurement frequency and bias sweep speed was 1M Hz and 100mV/s, respectively. 27W of black light lamp was used as the UV light source.

3. Results and discussions

Measurement method of ϕ_{S_MIS}-V_G relationship

In the first place, the depletion capacitance(C_D) was exclusively determined by the semiconductor surface potential (ϕ_S) for the fixed doping profile. Here, the ϕ_S is defined as the potential difference between surface conduction band edge and Fermi level. In the C-V measurement of SBDs, C_D is the measured capacitance and ϕ_S can be easily calculated from gate voltage (V_G). Therefore, the C_D-ϕ_S relationship can be directly measured from the SBDs. Then, from the C-V measurement of MISD, the depletion capacitance of MISD (C_{D_MIS}) can be calculated from $1/C_{MIS}(V_G)=1/C_{OX}+1/C_{D\_MIS}(\phi_S)$, where C_{MIS} is the total capacitance of the MISD and C_{OX} is the SiO_2 capacitance. This C_{D_MIS} can be used to determine ϕ_{S_MIS} from the ϕ_S-C_D relation of the adjacent SBDs. Then, the ϕ_{S_MIS}-V_G relationship for MISDs can be obtained without ideal MISD curves.

Measurement at high temperature (150℃)

Dashed lines in Fig. 2 showed the curves for the MISDs measured at 150℃ without illumination. At 150℃, the capacitance has a flat region between –2V and 4 V when V_G was swept from negative to positive voltage. E_C-E_F value for this region was 0.7~0.9eV. From this result, the flat region is not due to the hole inversion layer, but may be due to the I/S interface traps. However, the flat region did not appear in the V_G scan from positive to negative bias (from accumulation to depletion), but appeared in the opposite scan. During the scan from accumulation to deple-

tion, the negatively charged traps emit electrons, which will take a longer time from SRH statistics. On the contrary, in the opposite scan, the I/S interface traps capture electrons of the n-layer as ϕ_S decreases, which will be faster. The pinned ϕ_S of 0.7~0.9eV does not necessarily indicate the I/S interface trap energy, but the capture time is fast enough when ϕ_S comes into this region.

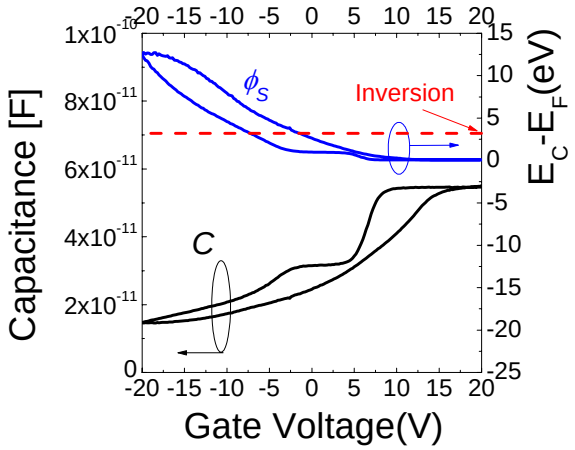


Fig. 2 C-V curves of MISD measured at 25℃ and 150℃ [Solid line (forward): 20V→-20V, Dashed line (backward): -20V→20V]

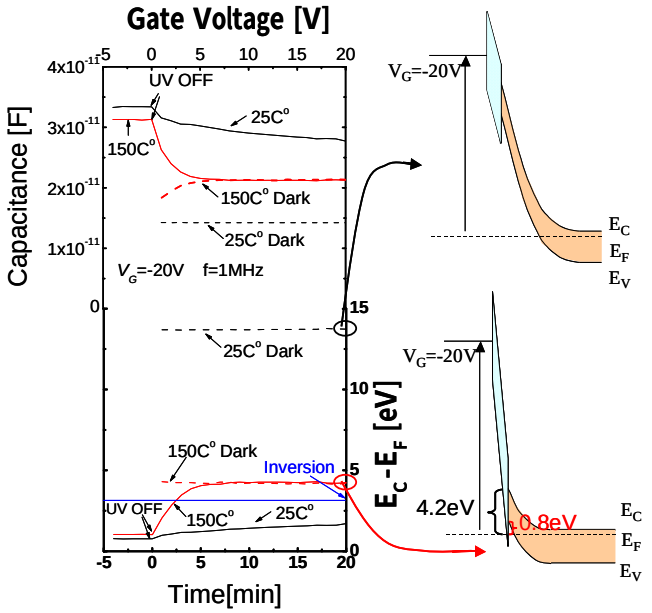
Time dependent Capacitance Measurement (-20V)

At 150℃ and 25℃, time dependent capacitance measurements at -20V were performed with and without illumination, as shown in Fig.3(a). Transient measurement was performed after 5min UV light illumination. The capacitance gradually decreased and finally reached a stable value, which is also the stable value obtained under dark condition. This indicates that the capacitance of the final constant value (C_{fnl}) is that for steady states. Comparing with SBD data, ϕ_S is 4.2V, which is much higher than the value for strong inversion condition. So, we should conclude that the hole quasi Fermi level and electron quasi Fermi level didn't coincide at the I/S interface, indicating that the thermal equilibrium is not established in the semiconductor, n-GaN.

The possible mechanism for the formation of this steady state will be the hole leakage through the insulator. Since the generation rates for wide-bandgap semiconductors are so small, that the generated holes will escape through the insulator before accumulating at the interface. To look deeper into this mechanism, we try to compare the generation rates of GaN and Si at 150℃ using the following equation:

$$U = -\frac{\sigma_n \sigma_p v_{th} N_t n_i}{\sigma_p + \sigma_n} \qquad [1]$$

where, σ_p and σ_n are the hole and electron capture cross section, respectively, v_{th} is the thermal velocity, N_t is the trap density. To roughly calculate the ratio of the generation rates for GaN and Si, we assume the same σ_p, σ_n, and v_{th} for GaN and Si while N_t(GaN) and N_t(Si) were 10^{20}cm^{-3} and 10^{15}cm^{-3}, respectively. Then the calculated ratio will be U(GaN)/U(Si)=4.73×10^{-9}, which is very small.



(a) (b)

Fig. 3 (a)Time dependent capacitance variation measured at –20V at 25℃ and 150℃ under dark condition and after UV illumination (Solid line: After 5min UV illumination, Dashed line: Dark) (b) Band diagrams of our MISDs for steady state at 25℃& 150℃

4. Conclusions

In conclusion, by thermal- and photo-assisted C-V measurements of n-GaN MIS diodes, we found high density of MIS interface states. The energy levels for the interface states were estimated to be 0.7~0.9 eV below the conduction band edge, but the accurate determination is difficult since the thermal equilibrium cannot be established in the MIS structure on GaN. The reason is that the leakage through the oxide is too large compared with the electron-hole generation rate in the wide band gap semiconductor.

For wide bandgap semiconductors, the insulator resistivity should be reexamined whether they are really acts as an insulator compared with the semiconductor resistivity and generation rate.

References

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