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Graphene Channel Field-Effect Transistors with Schottky Tunneling Source and Drain

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1. Introduction

Graphene as a channel material has been attracting much attention in recent years for CMOS applications because of its unique physical properties. A single layer graphene has a 2-dimensional system with hexagonal lattice structure where carbon atoms are connected with three neighbors and form sp^2 bonds. It is found to have extremely high mobility of around 15,000cm^2/Vs at room temperature [1], and has nearly ballistic transport in sub-micron range. Moreover, unlike 1-dimensional carbon nanotubes (CNTs), its 2-D nature makes it more compatible with planer CMOS technology.

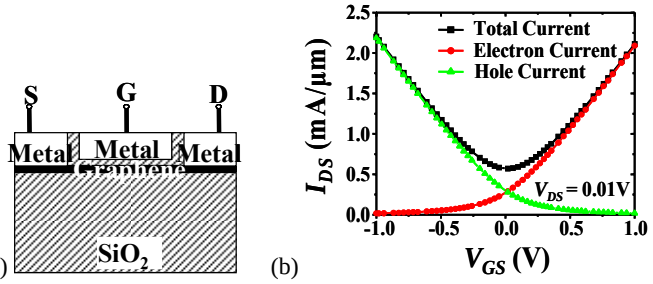
However, since graphene is a zero band-gap semi-metal with large electron and hole densities [3], it is difficult to deplete both of them in graphene at the same time. It is also known that graphene forms ohmic contacts with metals such as Ti, Cr, Au, etc. Therefore graphene channel Field Effect Transistors (Gra-FETs) with metal source and drain will show an ambipolar conduction. In other words, it will be very difficult to turn off the transistor. To suppress this ambipolar conduction, in this paper, Schottky tunneling junctions between graphene and polysilicon are formed at source and drain. In this way only electrons or holes will conduct the current so that ambipolar conduction is suppressed and therefore the transistor can be better turned off.

2. Device Simulation

Simulations were carried out using ISE-TCAD device simulator DESSIS. The schematics of cross-section of simulated structures are shown in figure 1(a) and figure 2(a). Monolayer graphene is used, with a thickness of 3.37Å [2]. Gate length is set to be 60nm, and the gate oxide has a thickness of 2nm. The ambipolar conduction of Gra-FETs with metal source/drain is clearly shown from the I_{DS}-V_{GS} curves in figure 1(b). The total current of the device is composed of electron current and hole current. This is because both electrons and holes are conducting current in graphene channel. As a result, the minimum current still has a relatively large value which makes it impossible to turn off the transistor.

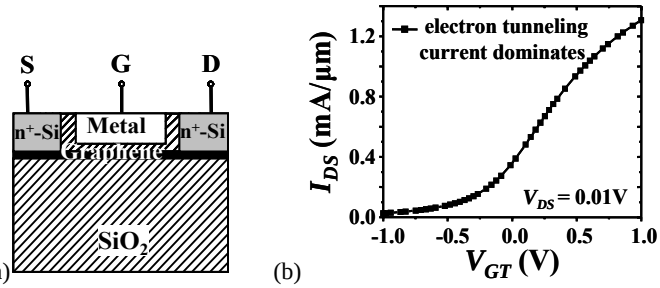
Applying Schottky tunneling junctions at source and drain will allow only one kind of carriers to conduct current. In other words, there will be only electron or hole current so that the ambipolar conduction could be suppressed.

Heavily n-doped PolySi is used to form Schottky junctions with graphene in the simulation. As graphene has a workfunction of 4.65eV [6], for the Schottky junction formed between n$^+$-PolySi and graphene, electrons will tunnel from source into channel but holes will encounter a large diffusion barrier. Furthermore, n$^+$ drain could only support few holes. By this method, the total current will be dominated by electron tunneling current. As shown in figure 2, unipolar conduction is realized and a higher I_{on}/I_{off} ratio is achieved.



(a) (b)

Fig.1 (a)Schematic of cross-section and (b) I_{DS}-V_{GS} Characteristics of Gra-FETs with metal source/drain in simulation.



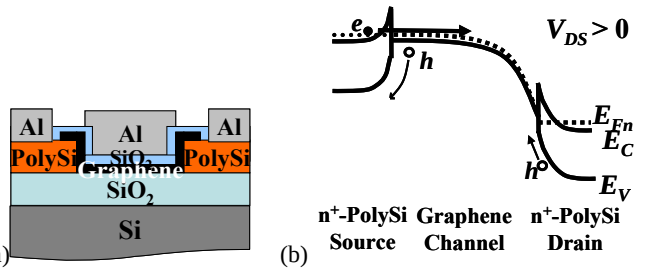
(a) (b)

Fig.2 (a) Schematic of cross-section and (b) I_{DS}-V_{GT} Characteristics of Gra-FETs with n$^+$-PolySi source/drain in simulation.

3. Device Fabrication and Discussion

Experiment

Graphene is produced from chemically converted reduced graphite oxide [5]. Top-gated Gra-FETs with PolySi source/drain are fabricated. As seen in figure 3(a), both n$^+$-PolySi and p$^+$-PolySi are deposited on 300nm SiO_2 substrate by LPCVD and patterned by normal lithography and dry etch. Graphene sheets are then spin coated on the substrate and SEM is used to identify where graphene is covering the channel area. After that, 20nm SiO_2 is deposited by PECVD and 500nm Al is deposited as top gate by e-beam evaporation and lift-off processes. Another 500nm Al layer is also deposited on top of PolySi in making source/drain contacts.



(a) (b)

Fig.3 Schematics of (a) device structure and (b) band diagram of Gra-FETs with Schottky source/drain

Top-gated Gra-FETs with metal source/drain are also fabricated as reference. Graphene sheets are first spin coated on 300nm SiO_2 substrate and Cr/Au metal contacts are deposited as source/drain by e-beam evaporation and lift-off processes. The same top-gate stack is deposited after SEM inspection.

Measurements and Discussion

As discussed in simulations, Gra-FETs with metal source/drain have ambipolar I_D-V_G conduction, which is clearly shown in figure 4. The solid line, as well as that in figure 5 and figure 6, is a fitting curve as a guide for eye. The total current is the sum of electron current and hole current. When electron current dominates (at large V_G), I_D increases with increasing V_G. When hole current dominates (at small V_G), I_D decreases with increasing V_G. As a result, the total current shows ambipolar behavior, first decreasing and then increasing with increasing V_G. We want to point out that because the chemically converted graphene is imperfect, the mobility is much lower than that was measured for ideal graphene [1], and thus the conduction of this film is worse.

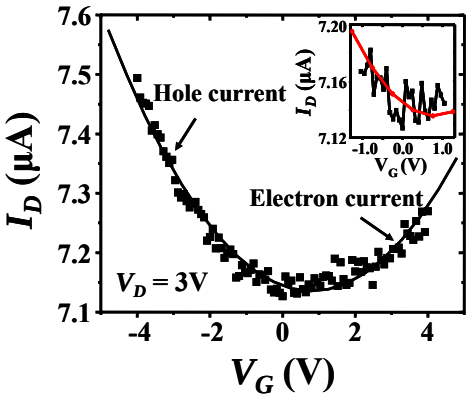


Fig.4 I_D-V_G Characteristics of Gra-FETs with Metal Source/Drain

Gra-FETs with n^+-PolySi and p^+-PolySi source/drain show different I_D-V_G relations, which can be seen in figure 5 and figure 6, respectively. Since graphene's workfunction is around the middle of silicon bandgap, it forms Schottky junctions with both n^+-PolySi and p^+-PolySi and has a tunneling barrier height of about 0.6eV. A schematic of band diagram along graphene channel contacted with n^+-PolySi source/drain is shown in figure 3(b). Gate voltage controls drain current by modulating electron density in graphene channel, and n^+-PolySi source/drain ensures only electrons tunnel through the barrier but not holes. Therefore the total current is dominated by electron tunneling current at all V_G region. As a result, I_D increases with increasing V_G. On the contrary, only holes will tunnel through the Schottky junction formed between p^+-PolySi and graphene so that the total current is dominated by hole tunneling current. Therefore I_D decreases with increasing V_G.

However the graphene film shows p-type behavior [5] which means it needs more positive V_G to convert. At V_G ranging from -1V to 1V, the majority carriers in graphene are still holes, as shown in the inset of figure 4. As a result, hole tunneling current is much higher than electron tunneling current. This explains why Gra-FETs with n^+-PolySi source/drain show much lower conduction, in figure 5. Additionally, recombination current may add to the small increase of total current at negative V_G.

Here for the first time, we proved experimentally that Schottky junctions formed at source/drain could act as filters to allow only one kind of carriers to conduct current.

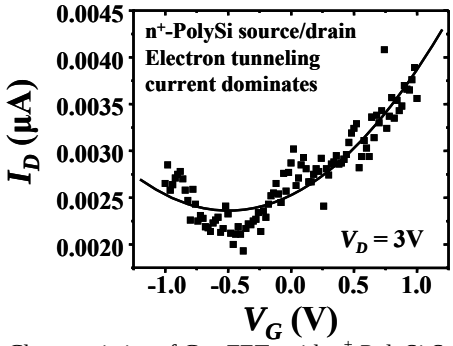


Fig.5 I_D-V_G Characteristics of Gra-FETs with n^+-PolySi Source/Drain

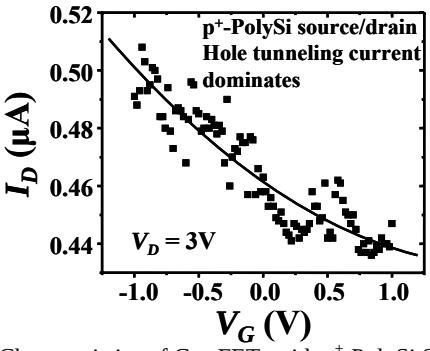


Fig.6 I_D-V_G Characteristics of Gra-FETs with p^+-PolySi Source/Drain

3. Conclusions

Using chemically converted graphene film, top-gated Gra-FETs with metal source/drain and Schottky tunneling source/drain are fabricated. Ambipolar conduction is observed for Gra-FETs with metal source/drain, because of the semi-metal property of graphene channel. Using heavily n or p doped PolySi as source/drain to form Schottky tunneling junctions with graphene successfully suppresses the ambipolar conduction. The total drain current is dominated by either electron or hole tunneling current and thus showing a unipolar relationship with V_G.

For the first time, we demonstrated the Gra-FETs with Schottky tunneling source/drain and proved experimentally that these devices would have only one kind of carriers to conduct current and thus the ambipolar conduction is suppressed.

Acknowledgements

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