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Charge transport in single and few layer graphene devices

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1. Introduction

Graphene-based materials are promising candidates for nano-electronic applications, ranging from high-speed circuits to single-molecule sensors [1-3]. One of the remarkable aspects of graphene, important for possible electronic applications, is the very high carrier mobility that can be achieved without the use of sophisticated material preparation techniques [1]. However, the carrier mobilities reported for single-layer and bilayer graphene are still less than those reported for graphite crystals at low temperatures, and it is currently unclear which layer thickness may be more suitable for a given application. For the optimization of future devices, it is important to understand how the electronic properties of graphene based materials evolve from those of Dirac massless particles in single layer graphene [1] to those of massive particles in bulk graphite as the number of graphene layers is increased. We experimentally address this question by investigating charge transport through single and few layers graphene as a function of carrier density, temperature, and perpendicular electric field.

2. Device and fabrication

Single and few layer graphene flakes are obtained by micro-mechanical cleavage of natural graphite crystals, and by their subsequent transfer onto a Silicon substrate covered by a 285 nm thick thermally grown SiO_2 layer. The thickness of the graphene layers is optically identified by analyzing the shift in intensity in the RGB green channel of the graphene flake relative to the substrate [4]. Subsequent Raman and transport measurements (quantum Hall, resistance dependence on a perpendicular electric field, etc.) confirm the validity of this optical method.

To generate a static electric field perpendicular to the graphene layers we use double-gated devices (see Fig.1): the highly doped Si substrate is used as back gate; the top gate is defined by means of electron-beam lithography and lift-off of electron-beam evaporated SiO_2 and of a Ti/Au bilayer.

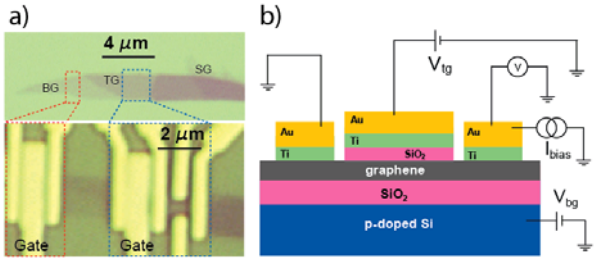

Figure 1 (a) Optical microscope images of an exfoliated graphite flake (top) containing single-layer graphene (SG), bilayer graphene (BG) and trilayer graphene (TG), and the devices (bottom) fabricated on the bilayer and trilayer parts of the same flake.
(b) Schematic diagram of a double-gated device. The position of the Fermi level in graphene and the applied perpendicular electric field are controlled by the voltages applied to the back gate (V_{bg}) and the top gate (V_{tg}). We study the resistance of the layers as a function of these gate voltages by applying an ac (f = 13 Hz) current bias I and measuring the resulting voltage V across the device with a lock-in amplifier.

3. Evaporated oxides as high quality top gate dielectrics

Key to the fabrication of top gated structures is the ability to deposit good quality thin gate oxides, with high breakdown field and low leakage current. We can routinely achieve high breakdown fields in electron-gun evaporated thin SiO_2 films (15 nm), comparable to the breakdown fields of thermally grown SiO_2, which is surprising giving that SiO_2 deposited by evaporation was long believed to be a poor quality insulator. To unveil the reasons behind the good insulating quality of our evaporated SiO_2 films, we conducted a statistical study of leakage current and breakdown voltage in capacitors, where two metallic electrodes are separated by a SiO_2 layer fabricated in different ways. We demonstrate that if the SiO_2 and the top gate metal electrode are deposited subsequently without exposing the SiO_2/metal interface to air, the electrical performance of electron-gun evaporated SiO_2 is comparable to that of thermally grown SiO_2. In contrast, exposure to air of the

SiO_2 layer before deposition of the counter-electrode leads to worst insulating characteristics. Our findings indicate that extrinsic degradation -probably due to the absorption of humidity- has limited in the past the insulating quality of electron-gun evaporated SiO_2. Further experiments are pioneering the possibility of using high-K dielectrics as top gates for graphene devices. These oxides will allow to study the influence of the gate dielectric on the mobility of graphene (which is believed to be one of the limiting factors of graphene mobility).

4. Charge transport through double-gated graphene devices

To investigate the evolution of charge transport properties as a function of an external electric field applied perpendicular to a graphene layer, we have fabricated double gated device structures where the graphene sheet is sandwiched between a top and back metallic gate insulated by two dielectric films from the middle graphene sheet-see Fig. 1b. When opposite voltage polarity is applied to the top and back gate, the graphene sheet experiences a large external electric field (E_{ex}). In the double gated device configuration, we can monitor how the in-plane graphene transport properties change in response to a finite external electric field. We have embedded different thickness of few layer graphene in these double gated structures and we have studied the different electric field response.

Our experimental findings show that the overall electric field dependence of the square resistance of graphene (single- and few-layers) devices is a unique property specific of each number of layers. In particular, in all cases the resistance exhibits a maximum whose value and position in gate voltage depend on the voltage applied to the gate on which a fixed potential is applied during the measurement. When the external electric field increases, the maximum of square resistance (Rsq^{max}) changes in a unique way, respectively in a single layer Rsq^{max} is not affected by a finite electric field; in bilayers at low temperature Rsq^{max} increases by few orders of magnitude; in trilayers Rsq^{max} decreases with increasing electric field.

Transport measurements over a wide range of temperatures (from 50mK up to 150K) confirm the unique electronic properties of single, double and triple layer graphene. In bilayers the larger E_{ex}, the more pronounced is the temperature dependence of Rsq^{max}. At Eex = 0, Rsqmax is only weakly temperature dependent (as it is typical of zero-gap semiconductors), whereas at $E_{ex} \neq 0$ the observed behavior is the one typical of an insulating state. The temperature dependence of the resistance in trilayers is opposite to the one observed in bilayers, and it reveals that this material system is a semimetal with a finite overlap between conduction and valence band. Measurements at finite E_{ex} show that the band overlap decreases when increasing E_{ex}, achieving 100% modulation. Thus double gated device geometry lead to the discovery of the only known electric field tunable insulator, i.e. bilayer graphene, and of the only known electric field tunable semimetal: trilayer graphene.

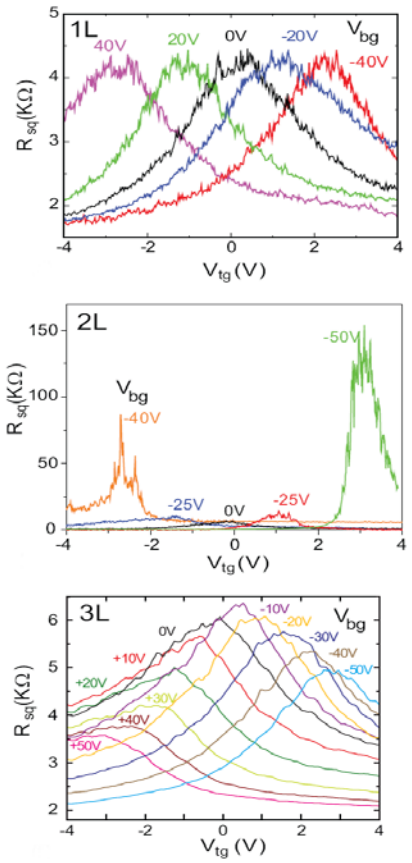

Figure 2. Plots of the square resistance in single (top), double (middle) and triple (bottom) layers respectively, measured while sweeping the top gates, for different fixed voltages applied on the back gate (for single and double layer T = 300mK,and for triple layer T = 50mK).

5. Conclusions

The ability to isolate and embed single- and multi-layer graphene in double gated structures is paving the way to reveal unique electronic properties of these systems. In particular, the metal-insulator transition reported in double gated graphene devices, introduces modern scientist to a conceptually new method of patterning graphene: double gated patterning. Our experiments demonstrate that top gating graphene is a non-invasive technology which leaves the transport properties (e.g. mobility) largely unchanged, therefore opposed to the invasive patterning by etching. Double gating technology holds the promise for changing the design concept of future applications based on graphene material systems.

References

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