Formation of High Ge concentration Virtual Substrate by Laser Annealing

C. Y. Ong\(^1\), K. L. Pey\(^1\), J. P. Liu\(^2\), Q. Wang\(^3\), C. P. Wong\(^3\), Z. X. Shen\(^3\), X. C. Wang\(^4\), H. Zheng\(^4\), C. M. Ng\(^2\), and L. Chan\(^2\)

\(^1\)Microelectronics Center, School of Electrical and Electronic Engineering, Nanyang Technological University.
\(^2\)Chartered Semiconductor Manufacturing Ltd.
\(^3\)Div. of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University.
\(^4\)Singapore Institute of Manufacturing Technology.

Phone: +65 67906371, Fax: +65 67933318, E-mail: eklpey@ntu.edu.sg

1. INTRODUCTION

SiGe alloy has been studied widely due to their extensive applications. Due to the smaller lattice mismatch with gallium arsenide (GaAs) as compared to Si, high Ge concentration Si\(_{1-x}\) Ge\(_x\) or pure Ge grown on Si substrate is used as a virtual substrate to integrate III-V materials [1]. In addition, Ge offers increased carrier mobility over pure Si. Ge and Ge-rich SiGe have been used in transistors to obtain high performance PMOSFETs [2]. It is very likely that these materials will be used for high performance CMOS technology beyond the 22 nm technology node.

High Ge concentration of Si\(_{1-x}\)Ge\(_x\) is likely to induce strain relaxation and dislocation propagation, which will result in the devices degradation. Graded Si\(_{1-x}\)Ge\(_x\) has been proposed to minimize the dislocation nucleation and propagation [3]. However, this is usually done by MBE or UHV-CVD, and the graded layer is very thick to minimize the threading dislocations [4]. In this paper, we propose to use laser annealing (LA) to obtain a thin graded Si\(_{1-x}\)Ge\(_x\) virtual substrate with high Ge concentration (~60%) at the near-surface region. Comparing with the sample annealed by RTA, LA shows the advantage of preventing the formation of large density defects at the Si\(_{0.8}\) Ge\(_{0.2}\)/Si interface.

2. EXPERIMENT

The process sequence for the Si\(_{1-x}\)Ge\(_x\) virtual substrate fabrication is shown in Fig. 1. The starting materials for the fabrication of virtual substrate are \(p\)-type B-doped Si (100) wafers. High quality of Si\(_{1-x}\)Ge\(_x\) films was grown on Si substrates by ultra high vacuum chemical-vapor deposition (UHV-CVD). The metastable films have a 50 nm uniform Si\(_{1-x}\)Ge\(_x\) with \(y \approx 23\%\), as shown in Fig. 2(a). Subsequently, a 30 nm \(\alpha\)-Ge layer was deposited on top of the Si\(_{1-x}\)Ge\(_x\) layer by electron-beam evaporation. The samples were then annealed by RTA at 950 °C for 30 s or by LA. LA was carried out in nitrogen ambient using a pulsed KrF excimer laser with a wavelength of 248 nm and a FWHM of 23 ns.

3. RESULTS AND DISCUSSION

Figure 2(a) shows the cross-sectional TEM (XTEM) micrograph of a Si\(_{1-x}\)Ge\(_x\) layer deposited by UHV-CVD. The metastable film is of very high quality and no observable defect is found at the interface, as indicated in Fig. 2(b).

For the sample deposited with a layer of 30 nm \(\alpha\)-Ge and RTA at 950 °C for 30 s, the XTEM micrographs show that the Si\(_{1-x}\)Ge\(_x\) film has been relaxed and dislocations are formed at the Si\(_{1-x}\)Ge\(_x\)/Si interface, due to the lattice mismatch between the Si\(_{1-x}\)Ge\(_x\) and Si (Figs. 3(a) and (b)). For the sample deposited with a layer of 30 nm \(\alpha\)-Ge and LA at 0.7 J/cm\(^2\) (10 pulses), two interfaces are observed, as shown in Fig. 4. From Fig. 5, the melt depth induced by the 0.7 J/cm\(^2\) LA is estimated to be ~65 nm by the simulation of the temperature profile using the heat transfer module of COMSOL Multiphysics. This explains the observation of two interfaces in the LA sample. The laser fluence of 0.7 J/cm\(^2\) is high enough to cause the whole \(\alpha\)-Ge layer and part of the Si\(_{1-x}\)Ge\(_x\) to melt. The Ge and Si atoms intermix at liquid phase and form a high Ge concentration Si\(_{1-x}\)Ge\(_x\) layer. The corresponding XTEM micrograph shows insignificant formation of dislocation at both Si\(_{1-x}\)Ge\(_x\)/Si\(_{1-y}\)Ge\(_y\) and Si\(_{1-y}\)Ge\(_y\)/Si interfaces (Fig. 4). SIMS data of the LA sample is shown in Fig. 6 and the Ge concentration extracted from SIMS is revealed (inset). The Si\(_{1-x}\)Ge\(_x\) layer has graded Ge concentration; Ge fraction varies from ~60% to ~23%. The graded Si\(_{1-x}\)Ge\(_x\) layer might play a significant role to prevent the high strain induced between the high Ge fraction Si\(_{1-x}\)Ge\(_x\) layer and the Si substrate, impeding the large amount of dislocations formation. In addition, the non-melt Si substrate acts as an effective heat sink, thus the cooling rate is too fast for the defect formation during the annealing process. As a result, no significant dislocation is observed at the two interfaces in this sample.

Fig. 7 shows the 532 nm Raman spectrum of the as-deposited sample and the samples annealed by RTA and LA. For the as-deposited sample, the Ge-Ge peak is broad, indicating the amorphous phase of this layer. Comparing Fig. 7(b) with Fig. 7(c), the Si\(_{1-x}\)Ge\(_x\)/Si\(_{1-y}\)Ge\(_y\) layer in the sample annealed by RTA has a higher average Ge concentration as compared to that annealed by LA. This can be shown by the higher Ge-Ge to Si-Ge peak intensity ratio for the sample that undergone RTA [5]. The reason is because 950 °C is insufficient to melt the Si\(_{1-x}\)Ge\(_x\) layer and hence it reduces the intermixing between the Ge and Si\(_{1-y}\)Ge\(_y\) layer.

4. SUMMARY

High Ge fraction Si\(_{1-x}\)Ge\(_x\) virtual substrate fabricated by LA has been demonstrated. The graded Si\(_{1-x}\)Ge\(_x\) formed by LA helps to reduce the dislocation formation at the SiGe/Si interface. By depositing a thicker layer of \(\alpha\)-Ge, it is possible to obtain a higher Ge fraction near the surface with low defect density by using LA technique.

References:
Laser annealing (LA) or 50 nm SiGe (23%) deposition by UHV-CVD 30 nm α-Ge deposited by e-beam evaporation

Fig. 1. (a) Process flow used for fabricating high Ge concentration Si_{1-x}Ge_{x} virtual substrate.

Crystallization

Rapid thermal annealing (RTA)

Fig. 2. (a) XTEM of a sample after the deposition of Si_{1-y}Ge_{y} on Si by UHV-CVD. Fig. 2 (b) shows the high quality and defect free at the interface of Si_{1-y}Ge_{y}/Si.

Fig. 3. (a) XTEM of a sample after a 30 nm α-Ge deposition and annealed at 950°C, 30s by RTA. Fig. 3 (b) shows a high density defects formation at the interface of Si_{1-y}Ge_{y}/Si.

Fig. 4. XTEM of a sample after a deposition of 30 nm α-Ge and annealed by LA at 0.7 J/cm², 10 pulses. No observable defect formed at the Si_{1-y}Ge_{y}/Si interface. The melt depth induced by LA is ~63 nm.

Fig. 5. Simulation of the temperature profile using the heat transfer module of COMSOL Multiphysics. The melt depth induced by LA at 0.7 J/cm² is estimated to be ~65 nm.

Fig. 6. SIMS profiling shows the Si and Ge atoms depth profile in the sample annealed by LA at 0.7 J/cm² for 10 pulses. The inset shows the Ge concentration extracted by SIMS.

Fig. 7. 532 nm Raman spectrum of (a) as-deposited sample; (b) sample went through RTA at 950°C 30s; and (c) sample went through LA at 0.7 J/cm² for 10 pulses. The peaks from the Si_{1-y}Ge_{y} layer in the as-deposited sample (a) are too weak to be detected.