Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp174-175

Low-dislocation-density 50nm Ge Fin Fabrication on Si substrate

Cheng-Ting Chung[1], Shih-Chiang Huang[2], Guang-Li Luo[2], Chih-Hsin Ko[3], Clement H. Wann[3], Hau-Yu Lin[3], Zong-You Han[1], Chao-Ching Cheng[1], and Chao-Hsin Chien[1,2]

[1]Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C.
[2]National Nano Device Laboratory, Hsinchu, Taiwan 300, R.O.C.
[3]Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan 300, R.O.C.
Tel: +886-3-5712121x54252, Fax: +886-3-5715506, E-mail: *chchien@faculty.nctu.edu.tw*

1. Introduction

Ge is considered an alternative material to enhance the device performance since it possesses both higher electron and hole mobilities than Si. For the feasibility of integrating Ge material onto Si CMOS platform, the heteroepitaxy technology of Ge on Si substrates is of high interest and it also provides the potential integration of optoelectronic function. Nevertheless, direct deposition of Ge on Si, in general, causes a considerable amount of misfit- and threading-dislocations (TDs) due to a large lattice mismatch (~4.2%). Several methods, Si_xGe_{1-x} buffer layers and high temperature annealing (HTA), have been reported to reduce the density of dislocation [1], [2]. Interestingly, a recent study proposed a new approach—the aspect ratio (AR) trapping, in which TDs can be effectively trapped at the bottom sidewall if using the oxide trench with the AR>1, thereby revealing defect-free Ge top layer [3]. In this study, we employed the nanoscale patterned growth with the cyclic HTA, to successively accomplish the low dislocation-density Ge fins on Si substrate.

2. Experimental

The standard shallow trench isolation processes were done on p-type Si(001) substrates with the patterned trench dimension of 650 nm × 50 nm. The wafer was dipped in diluted HF for 30s prior to Ge epitaxy in ultra high vacuum chemical vapor deposition (UHVCVD). At first, the chamber was ramped to 900 °C to prebake the sample for 10 min and then cooled down to 400 °C to grow Ge film at the pressure of 10^{-4} Torr (above steps were defined as one deposition cycle). Table 1 listed all the splitting growth conditions. We examined the epitaxial quality of Ge film through the transmission electron microscopy (TEM) and also estimated the dislocation area.

3. Results and Discussion

Figs. 1(a) and 1(b) show the cross-sectional TEM images of blanket samples #1 and #2, respectively. As seen, lots of TDs were observed for 1-cycle direct deposition of Ge [sample #1, Fig. 1(a)] and they can be efficiently eliminated by using the 3-cycle growth method [sample #2, Fig. 1(b)]. Through x-ray diffraction analysis (not shown), the values of the full width at half maximum showed an obvious decrease from 0.097 to 0.058 degree, while the measured Hall mobility increased from 325 to 1332 $cm^2V^{-1}s^{-1}$. These results gave a strong evidence of the improvement of Ge film crystallinity. Figs. 2(a)–2(c) show the TEM images of respective trench sample #3, #4, and #5, in which the cross-section is along the longer side (650 nm). In Fig. 2(a), lots of short TDs were observed in sample #3, similar to the results observed in blanket sample #2. With further decreasing deposition time to 2.5 hr per cycle for sample #4, TDs appeared mainly at the bottom and middle region of Ge film, as shown in Fig. 2(b). We reasonably speculate that separating the Ge growth into multiple deposition cycles, i.e., more times of HTA, assists to reduce the density of TDs through the gliding mechanism; also, HTA is added at the end should facilitate to repair the quality of whole Ge film. As displayed in Fig. 2(c), sample #5 indeed presents the almost TD-free Ge film and only somewhat dislocations gliding to SiO_2 sidewall were found. On the other hand, we also examined the dislocation distribution of these samples (#3, #4, and #5) along another side, i.e., 50 nm, as TEM images presented in Figs. 3(a)–3(c). Evidently, more reduction of defects was found, in particular unobservation of TDs in sample #5 [Fig. 3(c)] and we only characterized misfit dislocations at the Ge/Si interface from the plane-view TEM image (not shown). Figs. 4(a) and 4(b) summarize a statistical Weibull plot for the ratio of defect area to total area. As seen, for both directions in the trench, the percentage of defect area was reduced effectively through undergoing more cyclic HTA processes. Narrower trenches actually had the smaller defect density, which should be correlated to the lower formation probability of 90° TDs [4]. In Fig. 5, nano-beam diffraction analysis showed that the Ge fins were fully relaxed and the lattice constant close to Si surface was Si-rich SiGe alloy, arising from the interaction of surface Si atoms with Ge during HTA process.

4. Conclusions

In this work, heteroepitaxy of TD-free UHVCVD Ge fins on Si substrate has been accomplished through the use of nanoscale SiO_2 trench, accompanying the multi-step growth with the cyclic HTA. Such Ge/Si heteroepitaxy technique is of importance to realize the Ge FinFETs on the conventional Si platform.

References

[1] M. T. Currie *et al*., App. Phys. Lett., **72** (1998) 1718.
[2] M. Yamaguchi *et al*., App. Phys. Lett., **53** (1988) 2293.
[3] J.-S. Park *et al*., App. Phys. Lett., **90** (2007) 052113.
[4] G.-L. Luo *et al*., J. Electrochem. Soc. (unpublished).

Sample	Pattern	Cycles (Deposition Time per cycle)
1	Blanket	1-Cyc. (24hr)
2	Blanket	3-Cyc. (8hr)
3	Trenches	3-Cyc. (8hr)
4	Trenches	3-Cyc (2.5hr)
5	Trenches	5-Cyc. (1hr)+ 1-Cyc. (2.5hr)+ 900 °C HTA 10min.

Table 1 Splitting growth conditions.

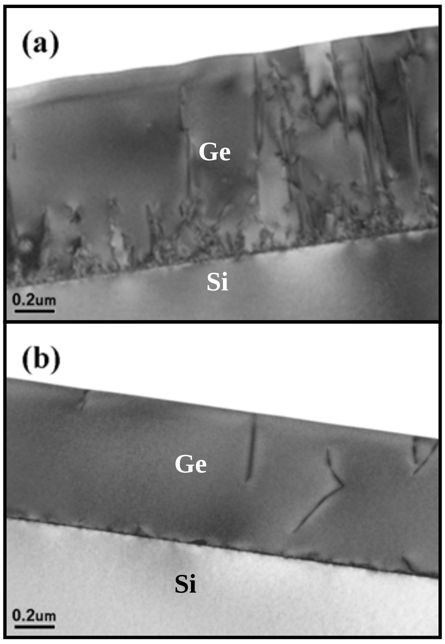


Fig. 1 TEM images of (a) 1-cycle growth and (b) 3-cycles growth. Total deposition time was 24 hours for both cases.

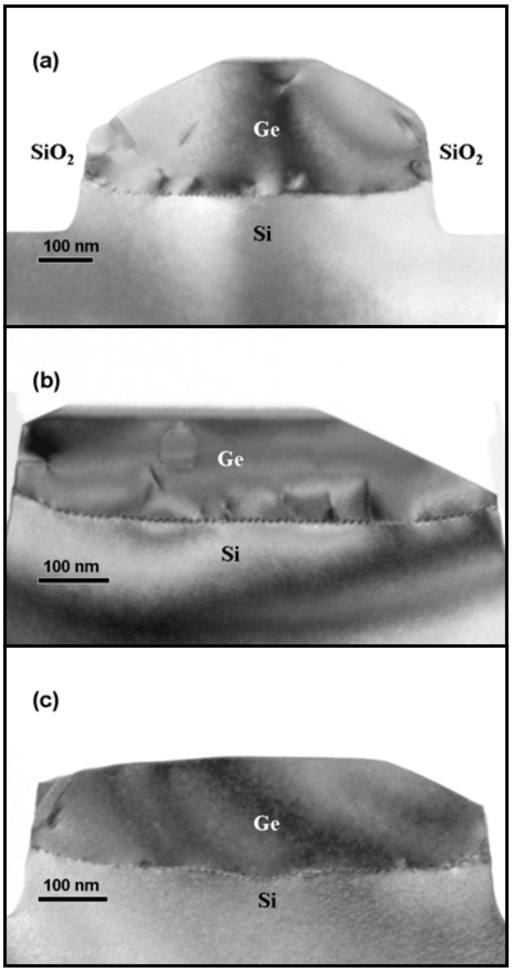


Fig. 2 TEM images of (a) 3-cycles (8hr dep. per cycle), (b) 3-cycles (2.5hr dep. per cycle), and (c) 5-cycles (1hr dep. per cycle) + 1-cycle (2.5hr dep. per cycle) + HTA. Note that the cross-section is along the longer side of the trenches (~650 nm).

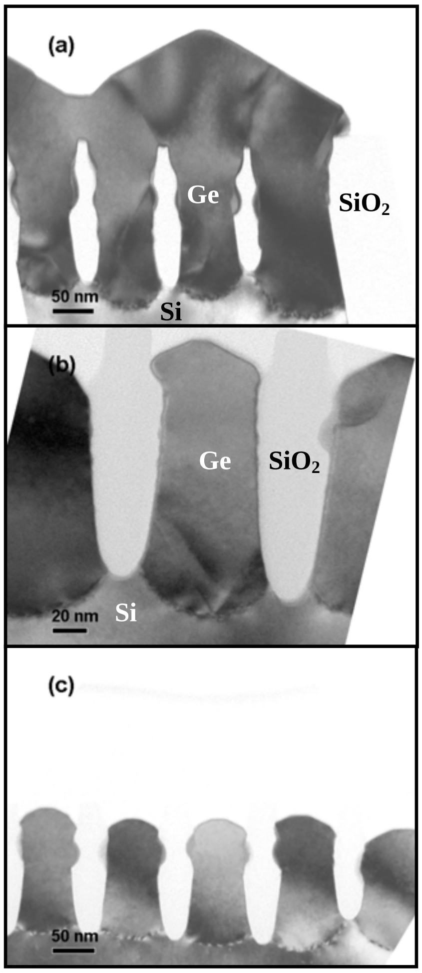


Fig. 3 TEM images of (a) 3-cycles (8hr dep. per cycle), (b) 3-cycles (2.5hr dep. per cycle), and (c) 5-cycles (1hr dep. per cycle) + 1-cycle (2.5hr dep. per cycle) + HTA. Note that the cross-section is along the shorter side of the trenches (~50 nm).

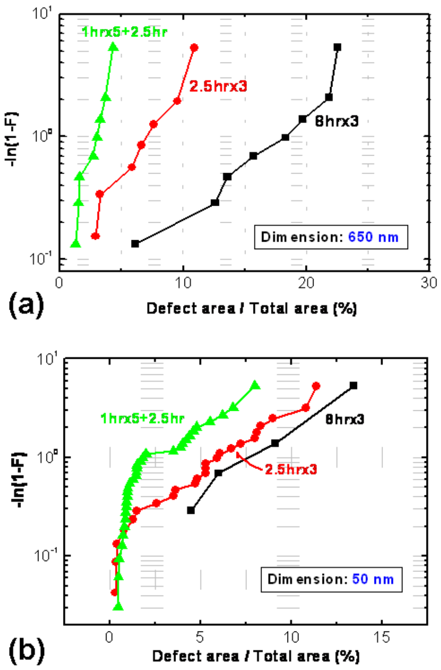
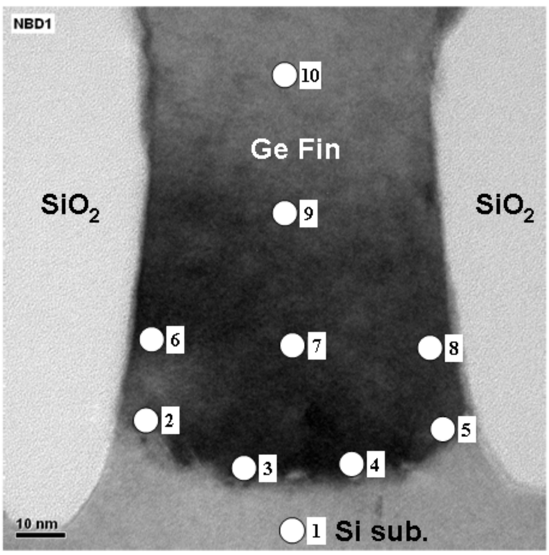


Fig. 4 Weibull plot of the ratio of defect area to total area for Ge fins within SiO_2 trenches along two different directions: (a) 650 nm and (b) 50 nm.



Point	Lattice Constant
Ge	5.646 Å
10	5.623 Å
9	5.645 Å
8	5.633 Å
7	5.630 Å
6	5.636 Å
5	5.430 Å
4	5.440 Å
3	5.560 Å
2	5.461 Å
1	5.431 Å
Si	5.431 Å

Fig. 5 Nano-beam diffraction analysis of Ge fin. Note that the diameter of electron beam is ca. 5 nm.