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Analysis of Hot Carrier Degradation for LDMOS under Gate Pulse Stress

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1. Introduction

BiC-DMOS [1] process is widely used for automotive ASIC, display driver and power supply management. Especially, LDMOS (Lateral Double diffused MOS) transistor is a key element for high power operation in this process. It is known that the degradation of LDMOS device under high power operation is suppressed by extending the accumulation region under the gate [2]. In addition, the self-heating phenomenon of LDMOS under high power operation should seriously influence on the reliability [3, 4]. However, there are few reports about the influence on the LDMOS device deterioration in the case that both the device structure and the junction temperature (T_j) are different. In this paper, we mention a hot carrier mechanism of LDMOS through detailed investigation using different device structure and different T_j.

2. Experiments

LDMOS transistors in this study are processed in the 0.25 μm SOI-BiC-DMOS technology [1]. Fig. 1 shows the schematic cross-section of LDMOS used in this study. The degradation of LDMOS under the hot-carrier injection is evaluated on the different lengths of N^- region under the gate, whose lengths are 1.0 μm (GT10) and 1.3 μm (GT13), respectively. Hot carrier degradation is evaluated at the condition of V_g = 7 V and V_d = 35 V, for a high power condition at the room temperature (T_a = 25 ^{0}C). Drain voltage is applied at DC mode, and gate voltage is applied at AC mode with pulse width of 1 μs. T_j of LDMOS device under high power operation is estimated by simulated thermal resistance and controlled by the duty of V_g pulse operation, as summarized in table I.

3. Results and Discussion

Fig. 2 depicts the dependence of V_{th} shift and Ids shift on T_j after the accumulated net stress of 1000s. It is noted that these shifts aren't influenced by switching stress in AC mode stress [5]. No difference of V_{th} shift can be seen between GT10 and GT13. Moreover, V_{th} shifts increase with increasing the T_j. On the contrary, the behavior of I_{ds} shift is quite different. I_{ds} shift of GT10 is larger than that of GT13. Furthermore, the dependence of the I_{ds} shift on T_j shows a small tendency. To clarify these phenomena, charge pumping measurement is carried out. Fig. 3 represents charge pumping current after the stress. The I_{cp} signal consists of two components of N^- region (V_{base} < -1V) and P-body region (V_{base} >-1V). The origin of V_{th} shift should be the interface state generation in P-body region. Therefore, the dependence of I_{cp} signal in P-body region on T_j and GT is shown in Fig. 4. I_{cp} shift of GT10 and GT13 are almost the same and T_j coefficient of I_{cp} shift shows a good agreement with that of V_{th} shift. It is found that V_{th} shift is attributed to the bias temperature instability, which is determined by the vertical electric field. Fig. 5 shows charge pumping current of LOCOS edge region after stress to analyze the I_{ds} shift. The $V_{g\text{-}low}$ for charge pumping measurement is relatively high to evaluate the LOCOS edge region, because the origin of I_{ds} shift would be interface state generation in this region. I_{cp} of GT10 is larger than that of GT13. Higher electric field at Bird's Beak (B.B.) region of GT10 structure produces the large amount of interface state. Moreover, the lower duty cycle, which corresponds to the lower T_j, results in large I_{cp}. It is expected that hot carrier is easily generated and injected as the temperature is reduced. The device simulation is carried out to clarify this phenomenon in more detail. Fig. 6 gives the estimated amount of hot electron and I_{cp} shift at B.B. region, which is obtained from the value at $V_{g\text{-}low}$ of –8 V in Fig. 5. Here, the amount of hot electron is calculated from electron concentration (ele.conc.) and probability ($P_{\Phi B}$) followed by Lucky-electron model [6]. The temperature dependence of various parameters is taken into account for the probability ($P_{\Phi B}$) that an electron will acquire an enough kinetic energy. The behavior of I_{cp} shift and hot electron should show same tendency. Moreover, both value show relatively small increase as decreasing the temperature T_j. The behavior of I_{ds} shift is explained by above discussion.

4. Conclusions

We investigate the dependence of hot-carrier degradation on junction temperature for two types of LDMOS, which has different N^- offset length, in detail. V_{th} shift according to the bias temperature mode is observed. On the contrary, the I_{ds} shift is influenced by the N^- offset length and a relatively small increase of I_{ds} shift is observed as decreasing the junction temperature. These phenomena are clarified by the charge pumping measurement and hot-carrier simulation.

Acknowledgements

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References

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Table I : Estimated junction temperature (T_j)

	Duty 10 %	Duty 25 %	Duty 50 %	Duty 100%
GT10	346 K	409K	498 K	631 K
GT13	347 K	412K	502 K	634 K

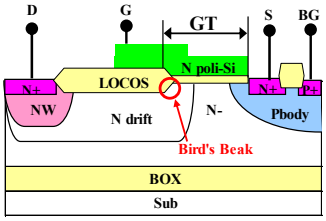

Fig1: Schematic cross-section of an LDMOS transistor

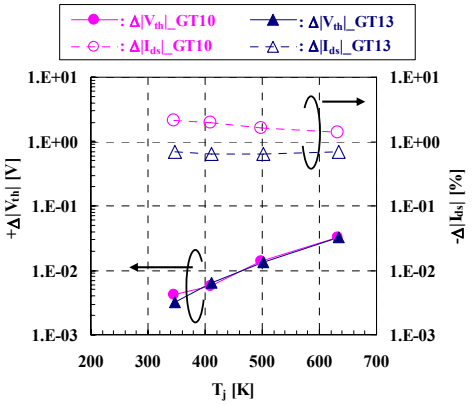

Fig.2: V_{th} shift and I_{ds} shift of LDMOS after the accumulated net stress of 1000s.

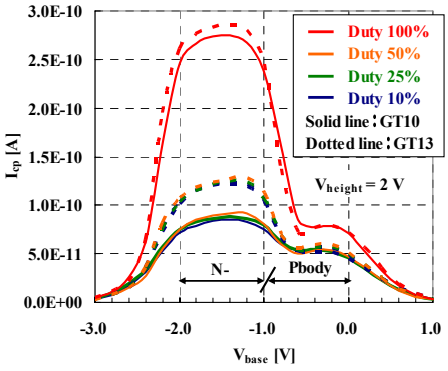

Fig.3: I_{cp}-V_{base} characteristics at V_{height}=2V after the hot-carrier stress with duty cycle as a parameter.

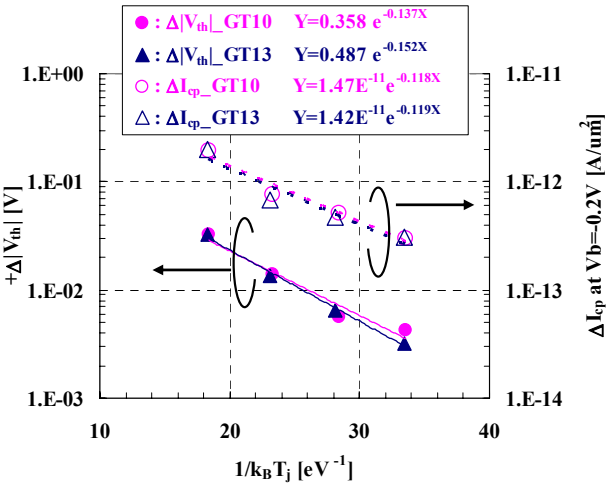

Fig.4: Dependence of V_{th} shift and I_{cp} shift on T_j at P-body region after the stress.

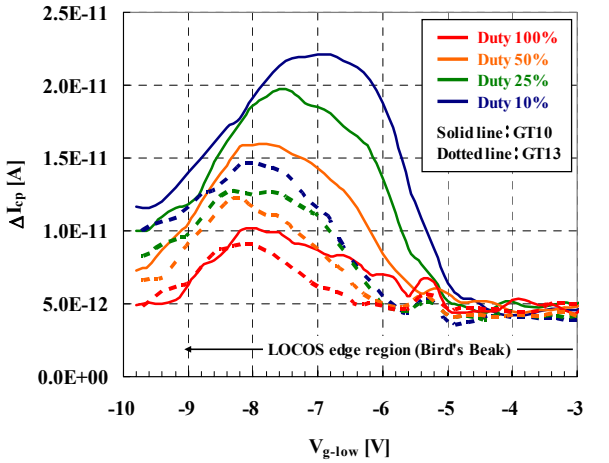

Fig.5: I_{cp}-$V_{g\text{-}low}$ characteristics of LDMOS after the stress with duty cycle as a parameter.

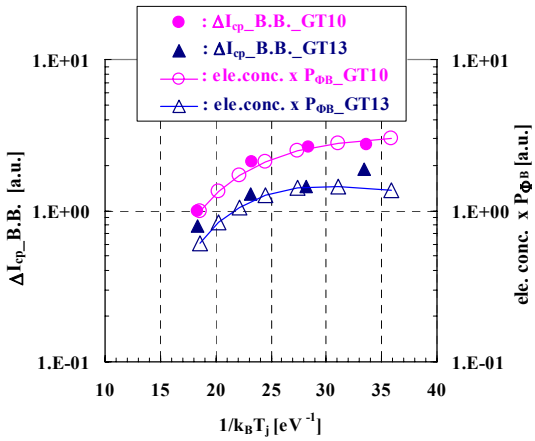

Fig.6: Dependence of I_{cp} shift and amount of injected hot-electron on T_j.