# **Current Distribution Analysis of IGBT Cells**

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# 1. Introduction

MOS controlled bipolar devices such as the Insulated Gate Bipolar Transistors are essential elements for today's power electronic systems. Parallel operation of IGBTs necessary to increase the current levels of the power modules have received much attention as their performances must be matched prevent current hogging and eventual breakdown [1-3]. However, to date, there is no report highlighting non uniformity of current distribution within an IGBT, arising due to RC propagation delay of the polysilicon gates.

Presently, a corner or a centred gate pad is employed in an IGBT with polycrystalline silicon gate material forming a RC network. This can result in the variation of the interconnect gate impedance between each cathode cells, which can influence their gate drive voltages. The resulting asymmetric current sharing during switching transients within the IGBT cells can cause limitation to the device operation due to current inhomogeneity and its resultant influence upon yield, maximum die-size, reliability and safe operating area (SOA) due to hot-spot. Therefore, for the first time, we investigate the influence of the gate impedance on the performance of a set of cathode cells of an IGBT. A simple analysis is presented using SABER to analyse its influence on the internal behaviour of an IGBT.

## 2. Model of IGBT cells in parallel

A simplified top view of an IGBT die is described in Fig. 1. For this stage, a 20A IGBT is considered, neglecting the area of the gate pad. The gate pad is considered at the centre of the chip. In this analysis, a simplified scheme of four cells located in a direct distance away from the gate pad is highlighted. Cells from other area of the chip and the under lying silicon structure are not discussed here as this article is focused on the effect of gate interconnection as the signal travels away from the gate pad. Neither is the influence of the device operation on the gate capacitance considered. Hence, the length from the edge of the gate pad to the centre of each cell is used to analyze the potential impedance within the interconnections.

The IGBT cell structure is shown in Fig. 2. All cells are assumed to have the same dimensions and identical parameters. Highly doped polysilicon is a commonly used gate material that propagates the gate voltage to all of the IGBT cathode cells within the chip. The resistance of gate pad area is neglected and the polysilicon conduction channel width is  $25\mu$ m. Therefore the resistance can be calculated from formula,  $R = R_s L/W$ , where R<sub>s</sub> is the sheet resistance of polysilicon, a typical value is  $1\Omega/\Box$ ; L and W are the length from the edge of gate pad to the centre of cell and width of polysilicon conduction channel respectively. The thickness of the underlying SiO<sub>2</sub> is 100nm.

The RC delay time [4] cross the conducting channel can be calculated and shown in Table 1. As the distance increases from the gate pad to cell location, the corresponding resistance and capacitance increases. The delay time increases as a function of the length of polysilicon are shown in Fig. 3. The gate voltage undergoes increasing delays as it travels away from gate pad, which increases with polysilicon sheet resistance, as shown in Fig. 4. The sheet resistance of the polysilicon is changed from  $1\Omega/\Box$  to  $10\Omega/\Box$  and the interconnect gate resistance varies proportionally. The difference in delay time among cells enlarges with this trend.



Fig. 1 A simplified topology of IGBT cells with gate pad placed in the centre of the chip. (The size is not scaled)



Fig. 2 Simplified structure of a typical 1200V planar IGBT

Cell	Polysilicon length(µm)	Resistance $(\Omega)$	Capacitance (pF)	Delay time(ns)
cell 1	562.5	22.5	4.86	0.109
cell 2	1687.5	67.5	14.6	0.983
cell 3	2812.5	112.5	24.3	2.731
cell 4	3937.5	157.5	34.0	5.354

Table I Calculated polysilicon resistance, capacitance and RC delay time (Rs= $1\Omega/\Box$ )



Fig. 3 The gate voltage delay time increases with the length of polysilicon (Rs=1 $\Omega/\Box$ ).



Fig. 4 The variation of the interconnection delay times with the sheet resistance of the polysilicon

### 3. Simulation of IGBT cells

The model of IGBT cells and parameters from Table 1 are imported into SABER [5] to simulate their switching behaviour. Fig. 5 indicates the normalised current distributions in percentage of the steady state current between cells at both turn-on and turn-off transients. Their current magnitudes show a decreasing trend during turn on and the opposite during turn off from cell1 to cell4 due to the delay between gate signals. These currents converge after the transient is complete.

#### 4. Conclusions

The interconnect delay between parallel of IGBT cells are analysed and estimated. It can be deduced that as the dis-



Fig. 5 The normalised percentage of transient peak currents against steady state value. (Rs= $1\Omega/\Box$ )

tance away from the centre gate pad to IGBT cell increases, the internal polysilicon resistance as well as the interconnect capacitance increases.

The resulting influence of the gate interconnect delay on the switching behaviour of the cells has confirmed through SABER simulations. The difference in parasitic resistance and capacitance from gate pad to IGBT cells can be considered as a major factor that influence the current balancing problem across the IGBT cells. These parameters are varied from cell to cell by the difference distances away to the gate pad. Also, this inhomogeneous current distribution will increase with the increase in device temperature. Further investigation of the chip topology design is needed to best avoid these problems.

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