Silicon Carbide Wafer Technologies for Power Devices

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1. Introduction

Silicon carbide (SiC) is a potentially useful material for power devices of high temperature and high power density power electronics system, due to its wider band-gap and higher electrical breakdown field than those of silicon. Several types of SiC devices, such as SBD, BJT, have already been available in the market, and SiC MOSFET is expected to be appeared soon. However, there are several issues on SiC wafer technologies, which should be solved and should be improved. In order to support a sustainable green energy society, SiC power devices are expected to use more widely and conventionally. In order to achieve it, SiC wafer technology and manufacturing are expected to be improved rapidly. Since common SiC power device structures are vertical, both of high quality substrate and high quality epitaxial layer are required for fabricating devices. Form engineering point of view, it is important to develop design technologies of SiC bulk single crystal growth, and SiC epitaxial process. In this presentation, the recent progress of both SiC bulk single crystal growth and epitaxial process for device layer would be summarized.

2. Bulk single crystal growth

SiC single is usually grown by sublimation inside a closed carbon crucible more than 2000K. By using numerical modeling, the effect of heat and mass transfer inside a crucible on the macroscopic quality of grown crystal such as growth rate and crystal shape was

investigated [1]. Then active control of grown crystal shape by modifying crucible geometry was demonstrated.

Some of SiC physical properties, such as an absorption coefficient with wave length and doping concentration dependences [2], lattice constants with doping concentrations dependence, were estimated numerically. With taking account of these physical properties, effects of heat transfer inside a grown crystal on the microscopic quality such as residual stress and dislocation densities were also discussed.

The other bulk growth process, such as high temperature chemical vapor deposition (HTCVD), Si-melt based liquid phase epitaxy, will be also mentioned.

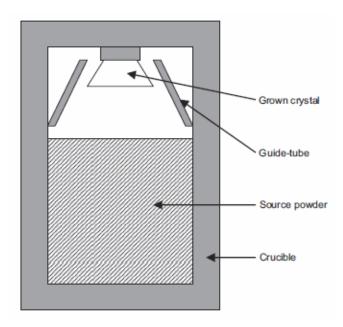


Fig.1 SiC Sublimation Growth

3. Epitaxial process

Hot-wall epitaxy is one of the key processes to fabricate SiC device layers. There are lots of experimental reports on SiC hot-wall CVD. However, each report mentioned the particular results that strongly depend on the experimental conditions and reactor design. In addition, the discussion with inlet condition such as source gas C/Si ratio, not the depositing surface condition, leads to the confusion. To overcome this situation, a numerical modeling is attempted [3,4]. The author has tried to make it clear that depositing surface condition might be a universal parameter of SiC CVD, and the numerical modeling could predict the growth rate, surface morphology and doping concentration by taking account of the depositing surface condition.

The conventional SiC epitaxial process is based on SiH4 and C3H8 source gasses. Recently, chlorine-based SiC epitaxial process has attracted considerable attention. It might enable to obtain more uniform doping profile on a wafer, which will be important as increasing a wafer diameter. It also produces high growth rate, which is valuable to fabricate a high voltage devices with thick epitaxial layer. [2]

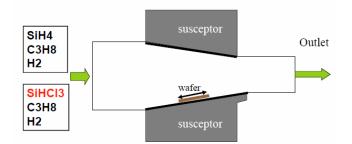


Fig.2 Simple 2D model for SiC-CVD process

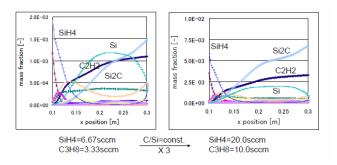


Fig.3 Gas-phase chemistry of SiH4-based CVD process

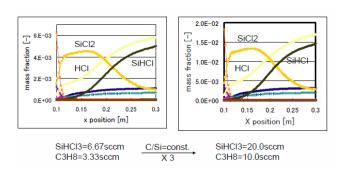


Fig.4 Gas-phase chemistry of chlorine-based CVD process

References

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