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Fabrication of InAs Nanowire Vertical Surrounding-Gate Field Effect Transistor on Si Substrates

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1. Introduction

Semiconductor nanowires (NWs), which are thin one-dimensional wire structures, are promising material for future device application such as field effect transistors (FETs), light-emitting devices, and so on. To build up such nanostructures, bottom up approaches utilizing growth technique are used. In particular, selective-area metal organic vapor phase epitaxy (SA-MOVPE) is a catalyst-free method and can control the size and position of NWs. Thus, it is expected to exhibit excellent properties and to offer wide variety of applications as compared to those grown in generally used vapor-liquid-solid (VLS) mechanism.

So far, many groups, including ourselves, have reported on the lateral NW-FETs [1-3] using NWs detached from grown substrates. However, it is difficult to control the position of devices and practical integration is almost impossible in such approaches. Thus, it is important to realize position-controlled NW array and use them in an as-grown form. This kind of approach also enable us to realize NW vertical surrounding-gate FETs (NW-VSGFETs), in which the gate is formed so as to surround the NW channel, leading to the suppression of short channel effects. To date, however, very few groups succeeded in their demonstration [4-6] because of difficulties in complicated three-dimensional processing.

III-V compound semiconductor materials and devices on Si substrate has attached great deal of attention because of their superior material property, for instance, high mobility, to realize high-speed and low-power consumption devices as well as of the possibility of integration with optoelectronic devices. One of the difficulties here is to overcome the lattice mismatching issues of heteroepitaxy which is inevitable in the conventional planar growth technology; however, with NWs having small foot print, it is thought to give a significant breakthrough on their integration on Si platforms. Recently, we have succeeded in the growth of periodic array of vertical InAs NWs on a Si substrate by SA-MOVPE [7].

Here, we describe the fabrication of NW-VSGFET using InAs NWs on Si substrates.

2. Experimental

2-1. SA-MOVPE growth of NWs

After thin SiO_2 film was formed on an n-type Si(111) substrate by thermal oxidation, periodic mask openings were formed by electron beam lithography and wet chemical etching. Then, InAs NWs were grown on the partially masked substrate in the low-pressure horizontal-MOVPE system, supplying trimethylindium (TMIn) and AsH_3 as source materials. Growth condition is as follows; partial pressure of TMIn, [TMIn] = 4.87×10^{-7}atm, partial pressure of AsH_3, [AsH_3] = 1.25×10^{-4}atm, growth temperature = 560°C, growth time = 20min. To realize vertical III-V NW array on Si substrates, special care was taken to prepare As-terminated (111) surface on Si prior to the growth. Detail of the growth process is reported elsewhere [7]. Figure 1 shows typical InAs NW array grown on n-Si substrate. The length of the NW is 1.5um and their diameter is 100nm, which is almost the same as the mask opening size.

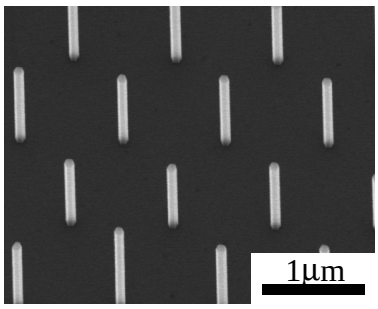

Fig. 1: SEM image of InAs NW array on Si substrate.

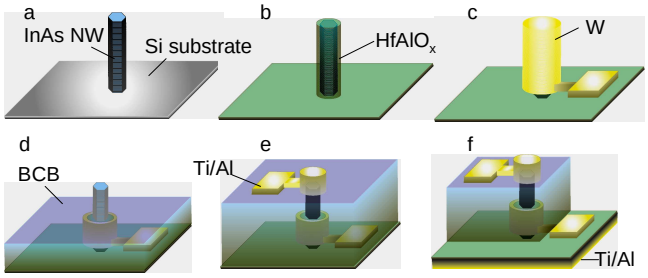

Fig. 2: Device fabrication process of NW-VSGFET.

2-2. Device fabrication process

Figure 2 summarize the fabrication process of NW-VSGFETs. After the growth (Fig.2-a), NWs were covered with high-k dielectric ($HfAlO_x$) by atomic layer deposition (ALD) for gate dielectric and for insulating layer between a substrate and a gate metal (Fig.2-b). Next, tangsten (W) was deposited as a gate metal by plasma sputtering and its contacting pad area were defined by photolithography process (Fig.2-c). To remove the gate metal and high-k dielectric resides on the top portion of NWs, protecting layer was formed with benzocyclobutene (BCB,

Dow chemical), which was firstly spin-coated and then etched back to the desired thickness by reactive ion etching (RIE) using O_2 and CF_4, followed by wet and dry etching of W (Fig.2-d). Figure 3-(a) shows an SEM image of the structure at this step. Note that this step determines the gate length of NW-FET, and was 500nm for the present structure. After that, the structure was spin-coated again with low-k BCB for the separation layer between gate and drain, and it was etched-back by RIE to expose drain region of the NWs. Ti/Al was evaporated on the top of the NWs for drain metal, and its contacting pad area was defined by photolithography(Fig.2-e). An extra BCB layer existing on the gate contacting pad area was removed by RIE at this step. Finally, source metal (Ti/Al) was evaporated on the back side of the Si substrate and rapid thermal annealing was carried out to obtain ohmic contact (Fig.2-f). Figure 3-(b) shows a schematic of device structure.

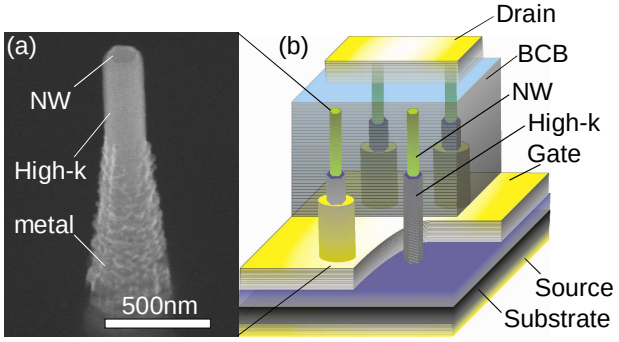

Fig. 3: (a) SEM image of device structure after gate process (b) Schematic of NW-VSGFET.

3. Results and Discussions

Electric characteristics of a NW-VSGFET were measured by using parameter analyzer (Agilent_4156). The results are shown in Figs. 4(a) and (b). Here these results are obtained with 50 NWs connected in parallel. Drain current was changed by gate voltages, showing successful demonstration of the characteristics of NW-VSGFETs. The FET is n-type with unintentionally doped InAs channel, as similar to many reports on InAs nanowire FETs. The threshold voltage is approximately 0 V, as shown in Fig. 4(b). Other characteristics as FET are summarized as follows: subthreshold slope, S = 1.87V/decade, peak transconductance, $G_{m,max}$ = 0.26mS (@V_G = 0.4V), on-off ratio, Ion/Ioff = 10^2.

We think following factors limit performance of our present NW-VSGFET and will be overcome by optimization. Firstly, we notice that the current-voltage characteristics between source and drain are asymmetric with respect to V_{DS} = 0. This is due to the band discontinuity at Si/ InAs NW heterojunction, where it is considered that electrons in Si see potential barriers across InAs. Such potential barrier results in the high access resistance at the source side of the channel, resulting in the suppression of drive current. To solve this issue, control of the doping both in substrate and NWs is required. It is also probable that there exist unexpected electrical conduction passes between source and drain which deteriorates the Ion/off values. This undesired NW passes should be easily removed by wet etching and lithographical technique. Other reason is in the quality of high-k dielectric. It is mainly affected by conditions of deposition, such as temperature, pressure, flow rate of precursor and post deposition anneal. Pre-deposition treatment is also important to control and minimize interface states at high-k/InAs NW interface.

To conclude, we reported on the fabrication of a vertical NW-VSGFET using position controlled InAs NW array grown by SA-MOVPE on Si substrate and demonstrated FET characteristics with n-type channel. Possible reasons limiting the present devices, such as band discontinuity at the Si/InAs interfaces, was discussed.

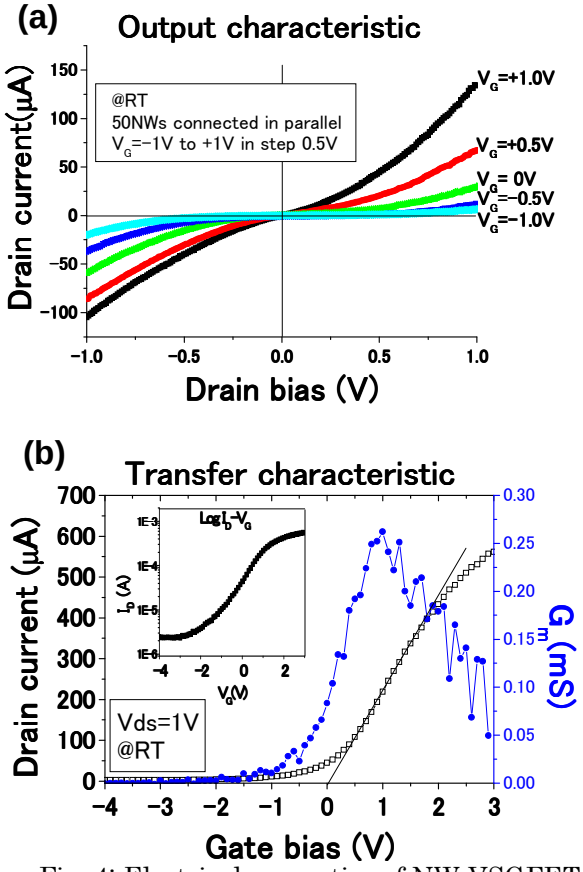

Fig. 4: Electrical properties of NW-VSGFET ((a): Output characteristic (b) : Transfer characteristic).

References

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