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Design and Fabrication of BDD-based Reconfigurable Logic Circuit on GaAs Nanowire Network

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1. Introduction

For development of future nanowire-based integrated logic LSIs, circuit architecture suitable for nanowire network structures is an important issue. In this paper, we investigate a novel reconfigurable logic circuit utilizing a semiconductor nanowire network together with binary-decision diagram (BDD) architecture.

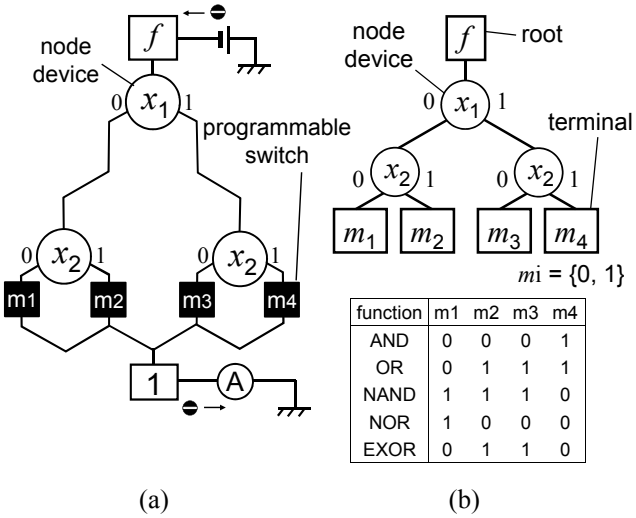
We have developed BDD-based logic circuits on semiconductor nanowire networks [1, 2]. Passive operation of the circuit enables to utilize various nanodevices. Previously we have formed a network representing a logic function by physically connecting or disconnecting nanowires. Here, as an alternative approach, a redundant nanowire network is formed and nanowire branches are connected or disconnected electrically. This paper describes a circuit design for any Boolean functions and demonstrates a two-input circuit using a GaAs etched nanowire network.

2. Concept and Design

Basic architecture of the present circuit is shown in **Fig. 1(a)**. It consists of a root, a terminal, node devices, and programmable switches. This circuit is possible to implement any combinational Boolean functions by programming the switches. For circuit design, a Boolean function is expanded using conjunctive canonical form. In case of two-input, for example, the function is expressed by

$$f(x_1,x_2)=m_1\cdot\bar{x}_1\cdot\bar{x}_2+m_2\cdot\bar{x}_1\cdot x_2+m_3\cdot x_1\cdot\bar{x}_2+m_4\cdot x_1\cdot x_2, \quad (1)$$

where m_i is a coefficient determining a specific function, taking value of 0 or 1. As shown in the table in **Fig. 1(b)**, various logics are obtained by suitable combination of m_i. Using a binary decision tree, the function can be represented graphically as shown in **Fig. 1(b)**. Then, a physical circuit is realized by transferring the logical graph structure to a physical nanowire network structure. Here, a network with hexagonal topology is chosen from the three-fold symmetry of the node device. Output is obtained by measuring current from the root to the terminal. When the current flows, the logic is true. The node device switches the path of the current according to input, x_i. The programmable switch represents m_i. It connects and disconnects a nanowire electrically when m_i = 1 and 0, respectively. By programming the switches, any combinational logic circuit can be realized on only a circuit. The circuit size can be decreased by reducing the tree using reduced-order BDD technique [3].



function	m1	m2	m3	m4
AND	0	0	0	1
OR	0	1	1	1
NAND	1	1	1	0
NOR	1	0	0	0
EXOR	0	1	1	0

(a) (b)

Fig. 1 (a) Circuit architecture of reconfigurable BDD logic circuit on nanowire network. (b) Binary decision tree representing complete set of two-input logic functions. Table shows example of logic functions and corresponding sets of m_i.

3. Experimental

Physical implementation of the present circuit is schematically shown in **Fig. 2**. GaAs-based etched nanowires are utilized for the physical network in this study. Schottky wrap gates (WPGs) are formed at each node to realize node devices. The programmable switch is designed by inserting a thin SiN layer between the gate metal and the nanowire. These simple structures are easy to fabricate and is useful to study the feasibility of the circuit. Other nonvolatile switches are also possible. The present circuit structure is obviously applicable to bottom-up nanowire networks.

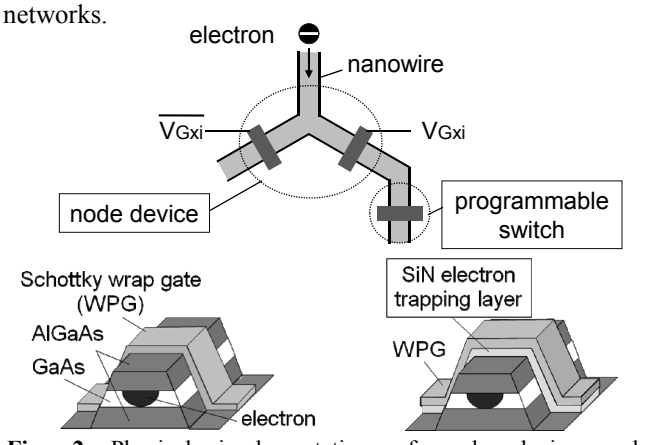


Fig. 2 Physical implementation of node device and programmable switch on GaAs nanowire network.

4. Result and Discussion

Fabricated two-input reconfigurable circuit is shown in **Fig. 3**. Nanowire width and WPG gate length were 500 nm and 300 nm, respectively. In this circuit, three node devices and four switches are integrated. Whereas, 42 transistors are required in a 2-input look up table of a standard Si CMOS design.

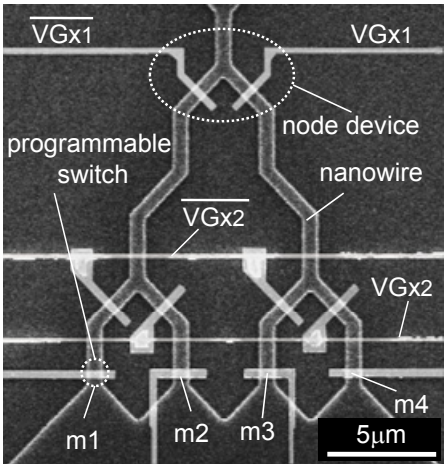


Fig. 3 Fabricated reconfigurable BDD circuit.

Figure 4 shows measured current switching characteristic of a fabricated programmable switch together with schematics for connect and disconnect states. Applying a positive voltage to the gate, electrons in the nanowire channel are captured in the SiN traps. Then, the nanowire is electrically disconnected and preserved. Applying a negative voltage, trapped electrons are erased and the nanowire is connected. The fabricated switch showed correct operation. Measured retention time was 20 ms at room temperature (RT), which was short but enough for circuit demonstration.

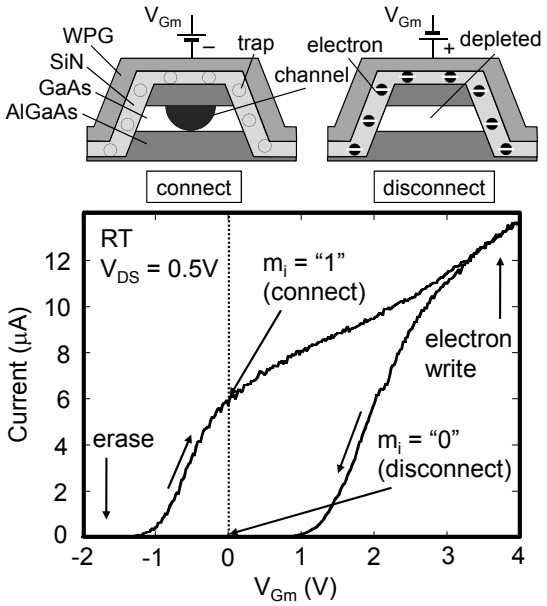


Fig. 4 Operation of a fabricated programmable switch.

Figure 5 shows measured input-output waveforms of the fabricated circuit programmed for NAND, OR, and NOR operations, respectively. In accordance with the table in **Fig. 1(b)**, m_i was programmed by applying suitable voltage to gates of the programmable switches for 1 sec. After programming, correct outputs could be obtained at RT. This result confirms the reconfigurable capability of the present circuit. Gradual change of the outputs was caused by the short retention time of 20 ms and unintentional electrical interaction between the switches. These problems will be solved by applying mature Si floating-gate FET technology and sufficient device isolation by suitable mesa etching [4]. Simple architecture as well as easy operation of the present circuits is favorable for nanowires and networks produced by various methods.

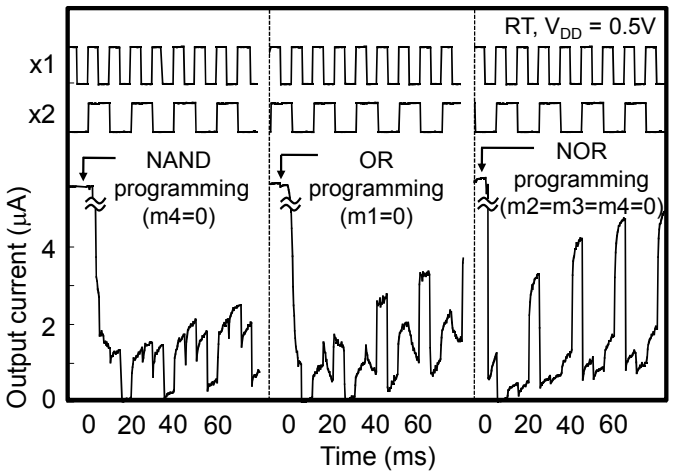


Fig. 5 Input-output waveforms of programmed to operate NAND, OR, and NOR circuit.

5. Conclusion

A novel reconfigurable logic circuit utilizing the nanowire network and the BDD architecture was investigated through the theoretical expression of the logic function and physical implementation. Two-input reconfigurable circuit was designed and fabricated using GaAs-based etched nanowire network and its correct multi-functional operation was demonstrated.

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