Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp924-925

Above-CMOS Inductor for Rapid Prototyping of Mixed-Signal SoCs

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1. Introduction

It has become general to integrate radio frequency (RF) circuits in a chip with large scale digital processing circuits as a system on a chip (SoC) [1]-[2]. In the RF circuit design, however, estimation accuracy of RF passive element characteristics is not enough as compared with the digital circuit design. Hence discrepancy between the simulated and measured results often occurs. If measurement results of test chip do not meet specifications, redesign and remaking of the chip are inevitable.

In this paper, we propose a novel prototyping method using above-CMOS inductors for the first time. It can reduce not only a development period but also cost of mixed-signal SoCs. Fabrication process and measurement results of above-CMOS inductors are presented. Furthermore, a voltage controlled oscillator (VCO) design with an above-CMOS inductor is also demonstrated.

2. Above-CMOS Inductor Fabrication and Measurement

Figure 1 shows the concept of the proposed prototyping method using above-CMOS inductors. In this method, on-chip spiral inductor is made on a CMOS integrated circuit chip separately after the normal manufacturing process to adjust the inductor parameters of each chip. The inductor parameters can be adjusted flexibly in chip-by-chip manner through simple processes. Experimental cut-and-try trials can be carried out many times with short turn around time. The proposed method can evaluate and adjust the RF circuit characteristics on the actual chip of mixed-signal SoC. This allows more accurate evaluation and prototyping.

Although we have developed several methods to form above-CMOS inductors, the *etching only* method shown in Fig. 2, which uses the top metal layer of the CMOS chip for above-CMOS inductor implementation, was utilized in this study. In this method, whole area where above-CMOS inductors will be placed must be filled with top-layer metal. Arrangement of vias to connect above-CMOS inductor to under-layer metal wires for feeding is also needed. Furthermore, the passivation layer on above-CMOS inductor areas should be opened. The *etching only* above-CMOS inductor formation was carried out as follows. Firstly, a CMOS chip fabricated with 0.18 μm CMOS process and diced into 5 mm x 5 mm die was pasted on a 2 inch silicon wafer for easy handling in later processes. Inductor shapes were patterned by just a one-time photolithography using PLA (parallel light aligner) with x1 mask. Then etching of top-layer aluminum and barrier-metal layer was carried out.

Symmetric type inductors and asymmetric type inductors were made with two different patterns, respectively. Figure 3 shows photomicrographs of inductor patterns before and after above-CMOS processing. Tables I and II list design parameters of fabricated above-CMOS inductors.

Above-CMOS inductors were measured over the frequency range from 10 MHz to 15 GHz. S-parameters measured by a vector network analyzer were converted into inductance and quality factor. As shown in Fig. 4, inductances depending on the shape of inductor were measured. The inductance of the symmetric type inductor at 1 GHz are 1.86 nH for chip 1 and 1.48 nH for chip 2. It varies about 20%. The inductance of the asymmetric type inductor at 1 GHz are 1.76 nH for chip 3 and 2.03 nH for chip 4. It varies about 15%. Though the quality factor also varies, there is no major degradation between two inductors with the same type.

3. Application of Above-CMOS Inductors to LC-VCO

A prototyping of an LC-VCO was demonstrated as one of the applications of above-CMOS inductors. The VCO schematic is shown in Fig. 5. Figure 6 shows photomicrographs of VCOs after above-CMOS inductor fabrication. The inductor shapes were the same as those shown in the previous section. Above-CMOS inductors having different parameters were successfully formed on different chips having the same underlayer CMOS circuits with chip-by-chip manner. Oscillation frequency was measured with a spectrum analyzer. Power supply voltage was 1.8 V. Measured tuning characteristics are shown in Fig. 7. Both VCOs using symmetric and asymmetric type inductors, oscillation frequency was respectively altered between two chips having different above-CMOS inductors. This indicates that the modification of circuit characteristics after conventional CMOS chip fabrication was successfully achieved by proposed above-CMOS inductor formation techniques. Each oscillation frequency corresponds with the value expected from the measured inductance of the above-CMOS inductor and capacitance of the varactor.

4. Conclusion

A novel prototyping method for RF mixed-signal SoCs using above-CMOS inductors has been proposed. Above-CMOS inductors were fabricated on CMOS chips in chip-by-chip manner by only photolithography and etching processes of top metal layer. Measurement results exhibited that the adjustment of the inductance was possible even after the CMOS chip fabrication. The inductance can be varied from 15% to 20%. The application of this technology to a VCO design was also demonstrated. We believe the rapid prototyping method using above-CMOS inductors described in this paper is the first realization of an experimental-based highly-effective prototyping scheme. We call it "*breadboard on a chip*" technology.

Acknowledgements

This research was supported by the Semiconductor Technology Academic Research Center (STARC).

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

[1] W. W. Si, et al., IEEE J. Solid-State Circuits. **43** (2008) No. 12, 2896.
[2] S. Lerstaveesin, M. Gupta, D. Kang, and B. Song, IEEE J. Solid-State Circuits. **43** (2008) No. 9, 2013.

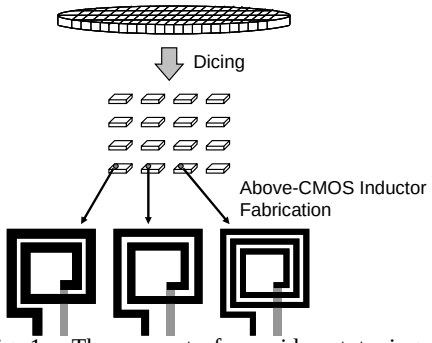

Fig. 1. The concept of a rapid prototyping of mixed-signal SoCs using above-CMOS inducotrs.

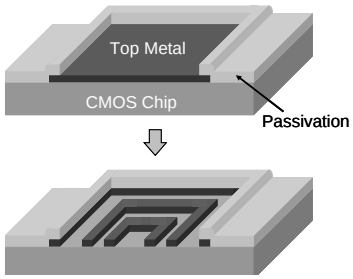

Fig. 2. Fabrication of the above-CMOS inductor.

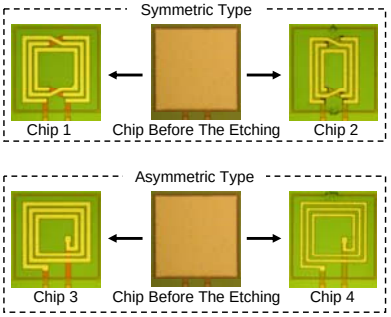

Fig. 3. Micrograph of fabricated above-CMOS inductors: symmetric type and asymmetric type.

Table I. Design Parameters of Symmetric Inductors.

	n	d (μm)	w (μm)	s (μm)
Chip 1	3	200 x 200	15	2
Chip 2	3	200 x 150	15	2

Table II. Design Parameters of Asymmetric Inductors.

	n	d (μm)	w (μm)	s (μm)
Chip 3	3	200 x 200	15	3
Chip 4	3	200 x 200	12	5

n: the number of turns, d: the outer diameter of the coil, w: the width of the conductor, s: the space between the conductor.

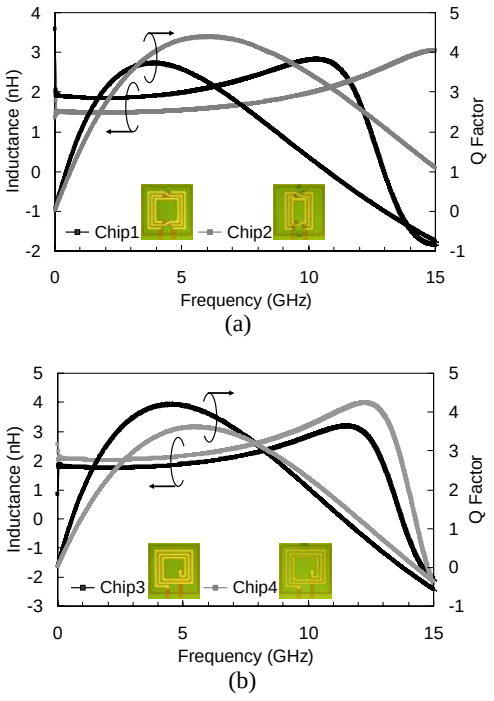

Fig. 4. Inductance and Q factor of above-CMOS inductors: (a)symmetric type, (b)asymmetric type.

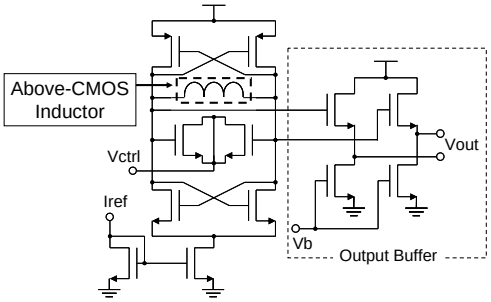

Fig. 5. VCO schematic.

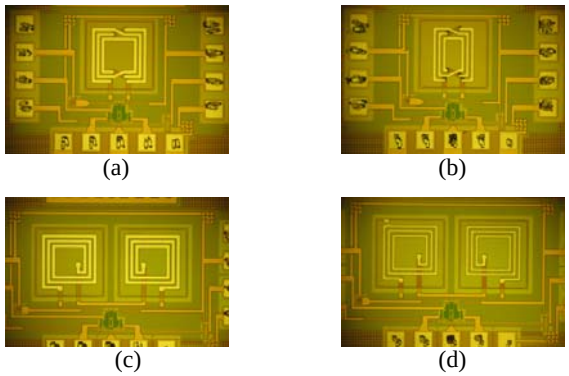

Fig. 6. Micrograph of VCO with above-CMOS inductors: (a)symmetric type of chip 1, (b)symmetric type of chip 2, (c)asymmetric type of chip 3, (d)asymmetric type of chip 4.

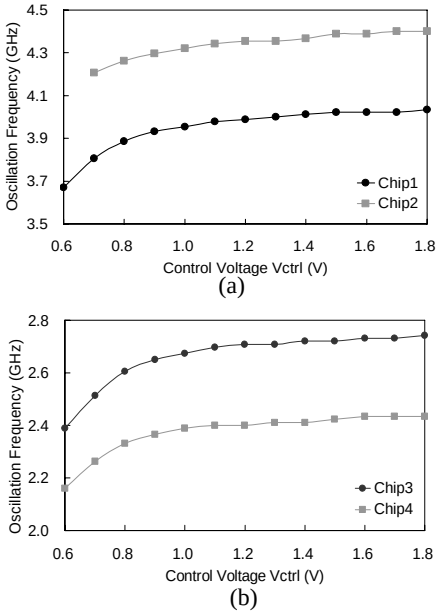

Fig. 7. Frequency tuning characteristics: (a)symmetric type, (b)asymmetric type.