Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp928-929

A New Differential-amplifier-based Offset-Cancellation Sense Amplifier (DOCSA) for High-speed SRAMs in Scaled-down CMOS Technology

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1. Introduction

Scaling of CMOS devices increases the performance variation, resulting in difficulty to achieve both area-reduction and speed-improvement for SRAMs simultaneously (Fig. 1). Namely, by scaling, delay in the peripheral logic parts decreases, while the worst-case bit-line (BL) delay increases due to the enhanced device variation. Increased BL delay results in an increase of overall access time of SRAM macros.

An effective way to reduce the BL delay is reduction in the offset voltage of a sense amplifier (SA). According to Pelgrom's wisdom, the offset voltage of a conventional latch-type SA can be reduced by increasing the gate width of input NMOS transistors [1]. However, this simultaneously increases the input capacitance of the SA, which is added to BL capacitance, negating the effect of BL-delay reduction. The conventional latch-type SA does not satisfy a target criteria of the speed (BL delay less than 1ns for 400MHz SRAM) and the area limitation. Therefore, an effective solution is reducing the offset voltage by using an offset-cancellation techniques (Fig.2).

In this work, we propose a new differential-amplifier-based offset-cancellation sense amplifier (DOCSA) for high-speed 6T-SRAMs with scaled-down CMOS technology.

2. Principle and Design of DOCSA

DOCSA consists of a single-stage differential amplifier with single-ended output, offset-compensation capacitors connected to its inputs, C_{OC1}, C_{OC2}, and CMOS switches. An operation sequence of DOCSA consists of four phases: 1) precharge, 2) BL-discharge and cancellation, 3) sense, and 4) latch (Fig. 3). The delay consists of the cancellation delay t_{cancel}, sense delay t_{sense}, and latch delay t_{latch}: t_{cancel} represents the settling time of the differential amplifier's output from applying negative feedback, t_{sense} the time from starting sense phase operation to the point at which the output swing of the differential amplifier exceeds the value of the offset voltage, t_{latch} the time from starting the latch operation to the output's reaching the CMOS logic level.

DOCSA uses a single-stage amplifier configuration and eliminates a latch stage by replacing it with the amplifier itself in a positive-feedback configuration, which keeps its area small. In addition, performing offset-cancellation operation during the BL discharge in SRAM read operation enables us to conceal the cancellation delay, keeping the total SA delay small. Here, the compensation capacitors are implemented with low-threshold voltage PMOS transistors.

We define offset-cancellation effect n is the ratio of the original offset voltage, V_{OS}, to the residual effective offset voltage, $V_{OS,eff}$, after the offset-cancellation operation (Fig. 4). The cancellation effect is dependent on amplifier gain. Therefore, poor amplifier gain degrades the offset cancellation effect. Moreover, charge-sharing between the compensation capacitances and the input capacitances attenuates BL-voltage difference by a capacitance ratio, degrading the cancellation effect. In addition, Miller effect in the differential amplifier worsens charge-sharing. Thereby, a cascoded-differential amplifier suppresses Miller effect, improving the cancellation effect.

3. Performances of DOCSA

We performed SPICE simulations and layouts with 40nm-node CMOS process technology. The best capacitance ratio of C_{OC1}/C_{IN1} and C_{OC2}/C_{IN2} determining a minimum delay in the target criteria is 4. At this capacitance ratio, the dependence of the cancellation effect on the gate length of transistors in the differential amplifier was estimated (Fig.5). There exists tradeoff relationship between the BL delay and the cancellation delay. At the intersection point of the BL delay and the cancellation delay, where the cancellation effect n=10 with L=0.066μm, a minimum delay is obtained. This point satisfies the target criteria, in which the area of DOCSA was ½ smaller than that of a conventional latch-type SA on the same offset voltage condition (Fig. 6).

To evaluate the cancellation effect of DOCSA, prototype chips were fabricated in 55nm-node CMOS process (Fig. 7). It is confirmed that distributions of the offset voltage were sharpened by DOCSA referred to the latch-type, especially for the FF corner. The offset voltage of DOCSA was 1/3 referred to that of the conventional latch-type SA. Further improvement is expected by using the cascode configuration in the differential amplifier.

4. Conclusions

A new offset-cancellation sense amplifier, DOCSA, is proposed to cure the device variation in scaled-down CMOS, suitable to use with high-speed and high-density 6T-SRAMs. The offset-cancellation effect was confirmed by the test chips fabricated in 55nm CMOS. Combination of CMOS scaling technology and deviation-relief circuit technology becomes important in advanced IT technology.

Acknowledgement

Authors acknowledge Drs. K. Takeuchi and H. Watanabe, NEC Electronics, for their kind advices and discussions.

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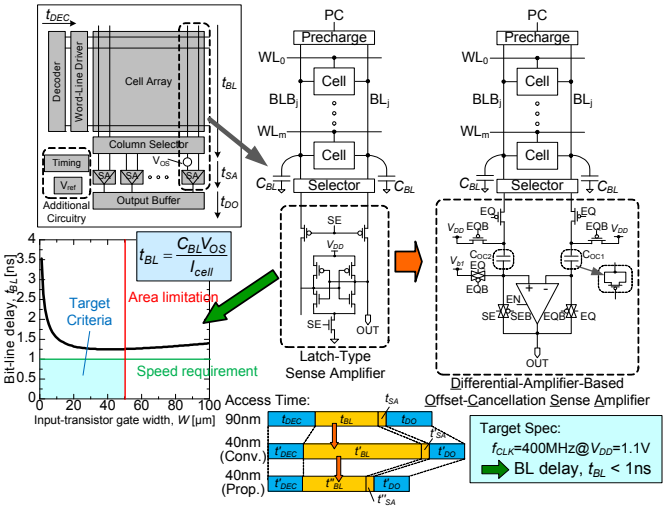
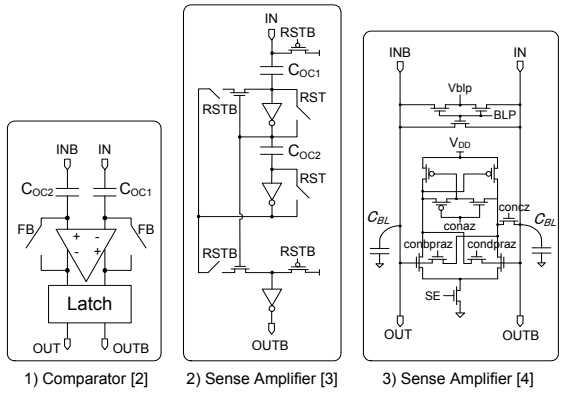


Fig. 1 Sense amplifier (SA) used for SRAM macro. A target speed of a high-density SRAM macro is 400MHz, which requires the BL delay less than 1ns. A conventional latch-type SA does not satisfy a target criteria because the BL delay cannot be reduced enough by increasing the gate width of input NMOS transistors. A proposed differential-amplifier-based offset-cancellation SA (DOCSA) reduces the BL delay by using an offset-cancellation technique, satisfying the target criteria.



Technique	Application	Advantages	Disadvantages
Comparator [2]	ADC	High gain	Large area, Low speed
Sense amplifier [3]	8T-SRAM	Small area, High speed	Less suitability to 6T-SRAM
Sense amplifier [4]	DRAM	Small area	Low speed
DOCSA (Proposed)	6T-SRAM	Small area, High speed	Low gain

Fig. 2 Comparison of three types of conventional offset-cancellation amplifier techniques and DOCSA. DOCSA has advantages of small area and high speed, but has a disadvantage of low gain. A high-density 6T-SRAM application requires high-speed sense amplifiers with small area, and does not require high-gain ones. Thus, DOCSA suits this requirement well.

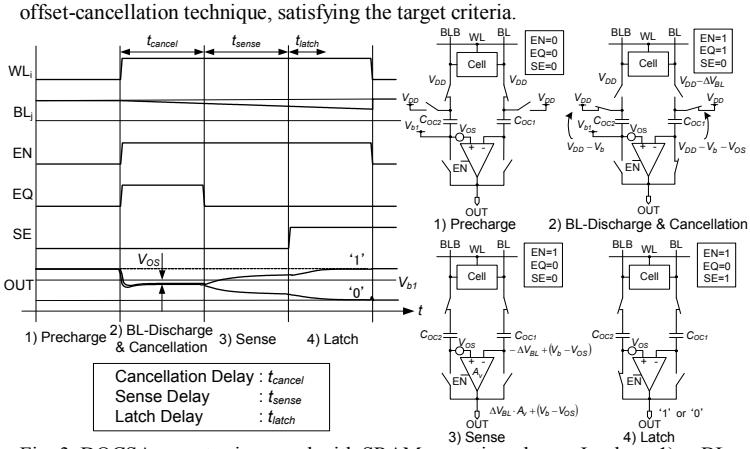


Fig. 3 DOCSA operates in accord with SRAM operation phases. In phase 1), a BL pair is precharged to V_{DD}. In phase 2), SA-inputs and BL-pair are switched off, and C_{OC1} is charged to reduce the offset with negative-feedback. A bias voltage V_{b1} is applied to the non-inverting input of the differential amplifier. In phase 3) the inputs of DOCSA are connected to BL-pair, and amplifies BL voltage difference. In phase 4), positive-feedback amplifies output swing to CMOS logic level.

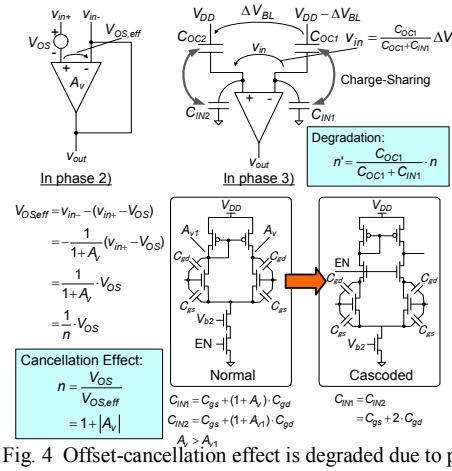


Fig. 4 Offset-cancellation effect is degraded due to poor differential-amplifier gain and charge-sharing between compensation capacitors and input capacitors. Miller effect in the differential amplifier worsens charge-sharing. A cascoded-differential amplifier suppresses Miller effect.

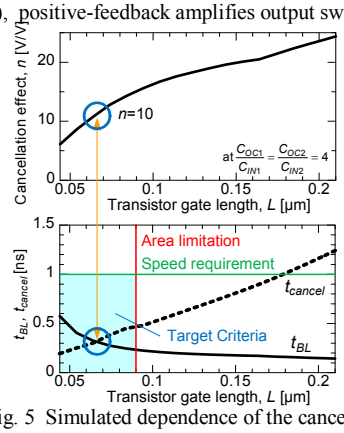


Fig. 5 Simulated dependence of the cancellation effect on the gate length of transistors constituting the differential amplifier with the capacitance ratio of 4 . Larger gate length makes the cancellation effect larger, which results in smaller BL delay, while requiring larger cancellation delay. A minimum delay is obtained at the cancellation effect n=10, satisfying the target criteria.

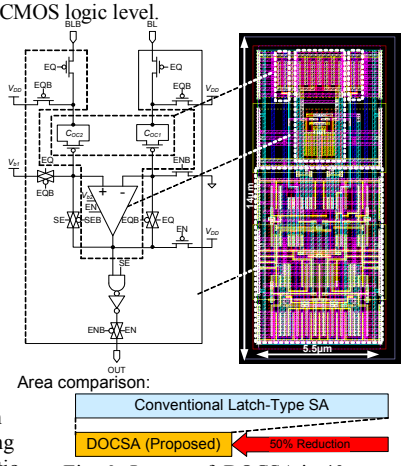
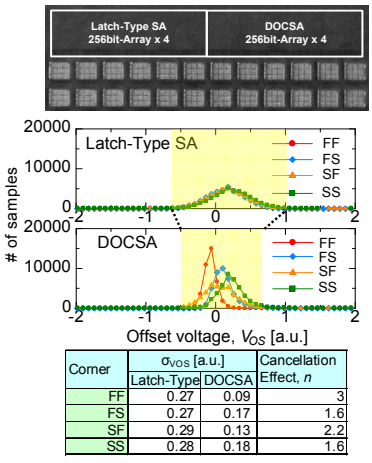


Fig. 6 Layout of DOCSA in 40nm CMOS. On the same offset voltage condition, the DOCSA area was half of a conventional latch-type SA one.



Corner	σ_{VOS} [a.u.]		Cancellation Effect, n
	Latch-Type	DOCSA	
FF	0.27	0.09	3
FS	0.27	0.17	1.6
SF	0.29	0.13	2.2
SS	0.28	0.18	1.6

Fig. 7 Measured offset voltage distributions of the conventional latch-type SA and DOCSA in prototype chips with 55nm CMOS. The distributions of the offset voltage were sharpened by DOCSA referred to the latch-type, especially for the FF corner.