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A 5 Gb/s CMOS photodiode with high responsivity of 2.49 A/W

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1. Introduction

The photodetector fabricated by standard Si CMOS technology is a good, low-cost approach for 850 nm wavelength optical communication. However, the low absorption coefficient of Si leads to low quantum efficiency (low responsivity) for a surface pn photodiode. The bandwidth is limited by the long transit time of slow diffusion photo-generated carriers in deep substrate. The former can be improved by using avalanche photodiode (APD) to increase the photo-generated carriers. The latter can be improved by fabricating PD on silicon-on-insulator (SOI) substrate or building PD on polysilicon layer [1]. However, in order to maintain the benefit of low-cost and high integration of CMOS technology, we implement photodetector in standard 0.18 μm CMOS technology without any modified process. In this study, we present an APD with body contact design to enhance bandwidth. The measured 5 Gb/s with 2.49 A/W is the best performance ever from a Si PD using standard Si CMOS process while biasing in the avalanche region.

2. Photodiode Design

Fig. 1 shows a three-diamensional (3-D) schematic structure of the proposed PD. A standard 0.18-μm CMOS mixed-signal process from United Microelectronics Corporation (UMC) is used in this design without process modifications. We fabricated the multiple p-n diodes in this PD design by using the n-well, p-well, shallow trench isolation (STI) oxide, and n/p implant from the standard process. The n/p implant are used for n- and p- type ohmic contacts, respectively. The STI oxide is used for forming isolation regions between active devices to reduce surface leakage and extend depletion region. Moreover, it can enchance breakdown characteristics and improve responsivity. When PD is operated in the avalanche region (at suitable reverse bias), the n-well, p-well and p-substrate region are depleted strongly and form a wide absorption region.

Additionally, the body contact design formed by p-implant and p-well is connected to the substrate. And it is around the active device like a guard ring to collect some of the slow diffusion carriers. The body contact metal is also provided to block the unwanted illumination into the deep substrate. Moreover, the metal-1 is designed to cover the whole chip area excluding the active area and pads. The active area is 50×50 μm^2. Fig. 2 shows two types of body contact designs. Fig. 2 (a) presents the body contact being connected to metal-1 (defined as ground), and Fig. 2 (b) shows the body contact being connected to metal-6 for possible different bias.

In order to reduce the long transit time of photocarriers, the n/p well and STI are placed at minimal distance defined by the process technology (design rule). The width for p-well, n-well, STI oxide is 1.5, 0.92, and 0.48 μm, respectively.

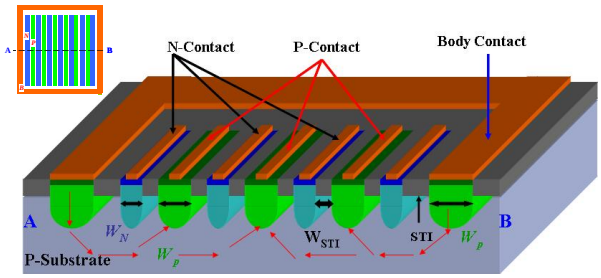


Fig. 1 A 3-D schematic structure of the proposed PD.

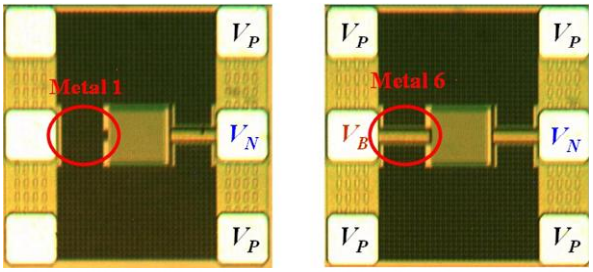


Fig. 2 Chip photo of two types of body contact design: (a) body contact is connected to metal-1/ground; (b) body contact is connected to metal-6/pad for biasing.

3. Measurement results and discussion

Fig. 3 shows the measured photo current, dark current, and responsivity for the PD with body contact grounded. Due to the body and p-well contact are connected to metal-1 (ground), the substrate is equivalent to ground. The PD shows a responsivity of 0.08 A/W at zero bias. At reverse bias(V_R) of 15.08 V (dark current is 1.84 μA), a higher responsivity of 2.49 A/W is observed from impact ionization. Fig. 4 shows the measured responsivity of the PD with different body voltages (V_B). Increasing the reverse bias of V_B decreases the responsivity slightly owing to a current path from the p-contact, through the substrate, to the body contact. A responsivity of 2.31 A/W is

observed at reverse bias of 13.32 V with V_B of -2V. The device in Fig. 4 exhibits an avalanche gain of over 20 at the onset of breakdown.

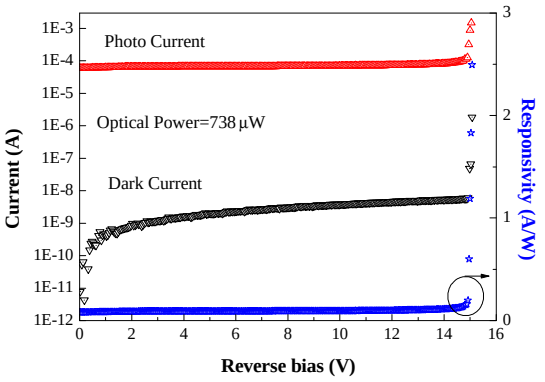


Fig. 3 Measured photo current, dark current, and responsivity of the PD with body contact grounded.

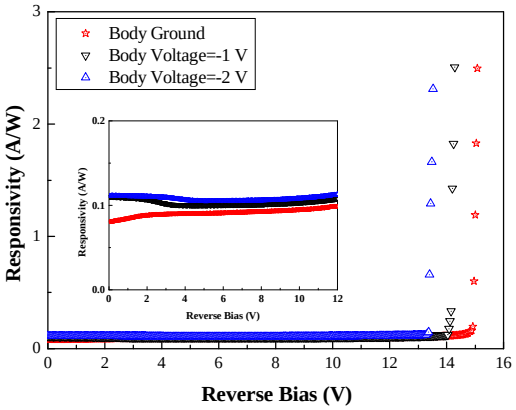


Fig. 4 Measured responsivity of the proposed PD with different body bias conditions. Inset shows the responsivity before avalanche.

Although supplying the body voltage leads to lower the responsivity, a higher bandwidth is observed due to the elimination of slow diffusion carriers from body current. In the measurement setup of 3-dB bandwidth, the 850-nm 10 Gb/s VCSEL is connected to one port and the PD is through the bias-tee connected to the other port of a 67 GHz vector network analyzer. As shown in Fig. 5, the PD achieves 3-dB bandwidth of 2.1 GHz at 15.08 V (body ground), 2.3 GHz at 14.28 V (V_B of -1 V), and 2.8 GHz at 13.52 V (V_B of -2 V). As observed, the electrical potential of the body bias takes effect. For eye diagram measurements, the PD is biased at 15.08 V with body ground and without connecting to any amplifier. Fig. 6 (a) shows that a data rate of 2.5 Gb/s meets the mask of SONET OC-48. The eye diagrams at a data rate of 5 Gb/s is also presented in Fig. 6 (b).

4. Conclusion

In this study, we demonstrate a high speed and high responsivity CMOS photodiode with body contact design. Under body ground, the PD achieves the bandwidth of 2.1 GHz and the responsivity of 2.49 A/W. Furthermore, the bandwidth of 2.8 GHz and responsivity of 2.31 A/W are observed at V_B of -2 V. The data rate of 2.5 and 5 Gb/s are also presented with PD biasing in the avalanche region.

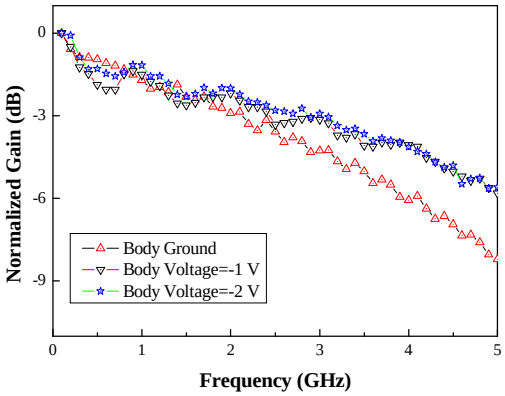
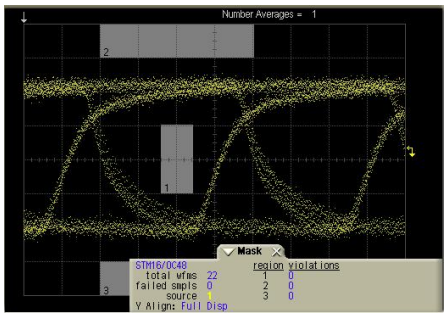
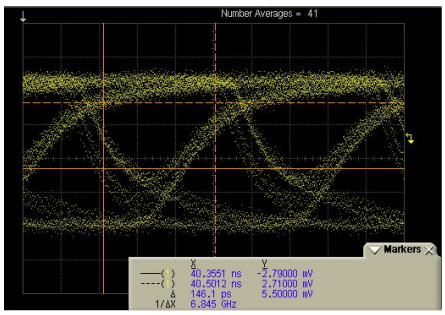


Fig. 5 Measured normalized frequency response of PD with different body bias voltage .



(a)



(b)

Fig. 6 Measured eye diagrams of Si PDs at data rates of (a) 2.5 and (b) 5 Gb/s without post-amplification.

5. Reference

[1] G. W. Neudeck, J. Denton, J. Qi, J. D. Schaub, R. Li, and J. C. Campbell, "Selective epitaxial growth Si resonant-cavity photodetector," *IEEE Photon. Technol. Lett.*, vol. 10, no. 1, pp. 129-131, Jan. 1998.