A high-responsivity of 4.1 A/W Si PD with BJT amplifier in standard CMOS process

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1. Introduction
Nowadays, integrated complementary metal-oxide-semiconductor (CMOS) PDs become popular in the application of near-infrared wavelengths (e.g. 850nm) due to its low cost, integration with receiver and systems-on-chip [1]. However, the low absorption coefficient of Si leads to low quantum efficiency (low responsivity) for a surface pn photodiode. The low responsivity can be improved by biasing Si PD in the avalanche region to increase the photo-generated carriers. In addition, many studies on the photodetectors made of Ge-related commercial process have been published in response to this demand. Polleux et al. [2] used a commercial SiGe BiCMOS process to fabricate an heterojunction photo-transistor (HPT) with a biasing base current of 60 µA. A responsivity of 1.49 A/W at 940 nm was obtained. Yin et al. [3] employed a commercial 0.25-µm SiGe BiCMOS process to realize an HPT. When the base current was biased at 5 µA, the responsivity for 850 nm light was measured as 2.7 A/W. When the base current was zero, the responsivity dropped to about 0.36 A/W.

In this work, we propose a new PD/BJT which is a Si PD with parasitic BJT amplifier fabricated in standard 0.18-µm CMOS process. A high responsivity of 4.1 A/W for 850 nm light was obtained while biasing PD/BJT in the avalanche range.

2. Device Design
The proposed device is to integrate a Si PD with parasitic vertical npn transistor in bulk CMOS process. The basic operation is similar to HPT which the base-collector junction diode is used for illumination and transistor is biased to amplify the photo-generated carriers. Fig.1 (a) shows cross section of a Si PD with parasitic vertical npn transistor. Fig. 1(b) shows the equivalent model and basic operation of PD/BJT. The Si PD is composed of multiple p-n diodes with shallow trench isolation oxide in between p- and n-region. The total active area of Si PD is 50×50 µm², which consists of nineteen p-n diodes. The npn BJT is formed by the n-diffusion, p-well, and deep-n-well structures. The emitter area of the npn BJT is 10×10 µm². An image of Si PD with BJT layout is shown in Fig.2. As shown in Fig. 1(b), n-contact of PD is connected with the collector of BJT and the p-connect is with the base of BJT. The emitter of BJT is grounded for 850nm illumination.

3. Characteristics of BJT and PD
The parasitic vertical npn BJT amplifier was characterized in the common emitter mode. Fig.3 shows the common-emitter I-V characteristics and demonstrates a high early-voltage. Fig.4 shows the current gain (β) from...
the measured Gummel plot. The measured β of BJT is about 20 for the collector current in the range of 1μA to 3mA.

The Si PD with p-n diodes leads to generate large number of photocarriers by operating at the avalanche range before breakdown. In the avalanche bias, the proportion of the photo-generated carriers in drift to carriers in diffusion is significantly increased and a higher bandwidth and responsivity can be observed simultaneously. In this case, the integrated BJT amplifies the photo-generated currents from the p-n diodes of Si PD and generates the output signal at the collector. Therefore, the responsivity is enhanced consequently.

![Fig.3 I-V characteristics of a 10×10 μm² BJT.](image)

![Fig.4 The current gain of a 10×10 μm² BJT. Inset shows the Gummel plot.](image)

![Fig.5 The measured dark currents of Si PD and PD/BJT.](image)

![Fig.6 The responsivities of Si PD and PD/BJT at 850nm.](image)

4. Conclusion

Without altering any step of the commercial 0.18 μm CMOS process, a high responsivity Si PD with BJT amplifier has been realized. The responsivity of the PD is improved from 0.37 A/W to 4.1 A/W while biasing at the avalanche range. Under the regular bias, the proposed PD/BJT demonstrates a high responsivity of 1.6A/W.

5. References