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Evaluation of GaN MOSFET with TEOS SiO_2 Gate Insulator

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1. Introduction

Semiconductor technologies will take important role to reduce the energy consumption by improving the efficiency of the electronic systems. Wide band gap semiconductor such as gallium nitride (GaN) has been approved to have the potential to develop high power and high efficiency device. In the field of power electronic, enhancement-mode (E-mode) is a key element to realize safe operation and reduce power consumption. To achieve this on wide band gap semiconductors, recently, MOSFET on GaN has attracted much attention to the researchers around the world. Even though the E-mode operation had been realized, however, the device performance such as channel carrier mobility is still low comparing with the silicon technology [1-3]. To improve the performance of the GaN MOSFET, effort is still necessary such as finding suitable insulator and improving their interface quality. In this paper, we will report the performance and characteristics GaN MOSFET with TEOS gate oxide and AlGaN/GaN heterostructure source and drain structure.

2. Device Design and Fabrication

The device structure is made on an AlGaN/GaN HFET structure with sheet resistance of 640 Ω/□. In this structure, the 2-dimensional gas (2DEG) layer is used as the Ohmic contact layer, and surface etched buffer layer is used as channel layer.

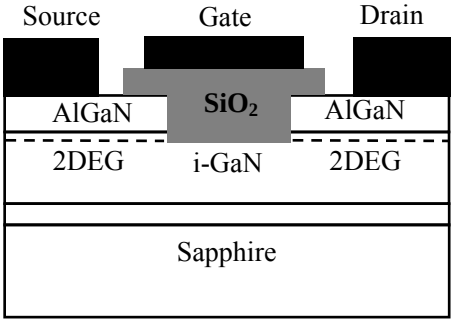

Fig.1 Device structure based on AlGaN/GaN HFET structure.

The fabrication process was based on the standard photolithography and lift-off technologies. As shown in Fig. 1, after device isolation by inductively coupled plasma (ICP) etching with $SiCl_4$ gas, the 2DEG layer in the channel region was also removed by the ICP using very slow etching rate to avoid etching damage. After that, a wet etching process with HNO_3:BHF=1:1 solution was followed to remove the possible contamination of Si on the etched surface. Next, plasma-enhanced chemical vapor deposition (PECVD, SAMCO PD-220) with liquid source of $Si(OC_2H_5)_4$ (TEOS) was utilized to form the SiO_2 insulator with the thickness of 70 nm. The ohmic contact was formed using Ti/Al/Ti/Au (50 nm/200 nm/40 nm/40 nm) with annealing temperature of 850°C for 1 minute in N_2 ambient. Evaluation by transmission line model (TLM) shows that the contact resistance is around 4.0 Ωmm. Finally, Ni/Au (70/30 nm) was deposited as the gate metal.

3. DC Characteristics

Device with gate length of 100 μm and gate width of 200 μm was used for device evaluation. The gate leakage current is shown in Fig. 2. The gate leakage current is below 10^{-10} A for the sample without HNO_3:BHF treatment, and 10^{-12} A for the sample with HNO_3:BHF treatment under gate bias from -6 V to 10 V. Unlike most of MIS HFETs, gate leakage is suppressed even at positive gate bias, which is the key for the enhancement mode operation.

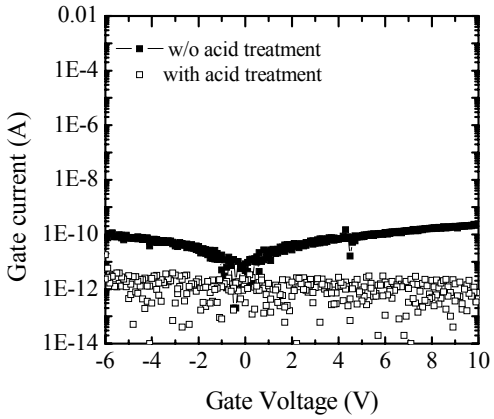

Fig. 2 The gate leakage current of the device.

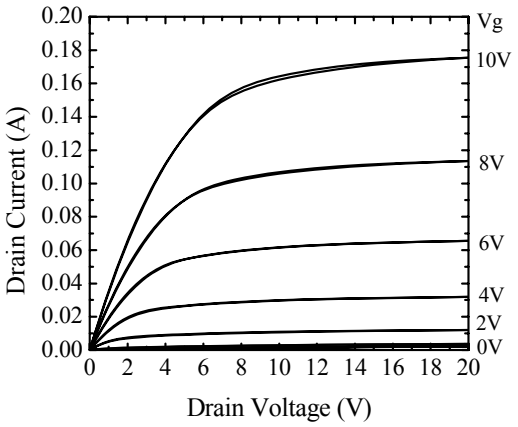

Fig. 3 The current-voltage characteristics of the device based on AlGaN/GaN HFET structure.

The current-voltage (I-V) characteristics of the device with HNO_3:BHF treatment is shown in Fig. 3. Near enhancement operation up to gate voltage of 10 V was confirmed. The transconductance is 0.36 mS/mm under gate voltage of 10 V and drain voltage of 20 V. Fig. 4 shows the transfer characteristics and the transconductance of the devices with and without acid treatment under drain voltage of 20 V. The subthreshold slopes, which were shown in Fig.5, are 1.19 V/decade and 2.79 V/decade, respectively, for the device without and with acid treatment. From the slope, the estimated interface state densities between SiO_2 and GaN are 9.3×10^{12}, 1.34×10^{13} /cm^2·eV , respectively.

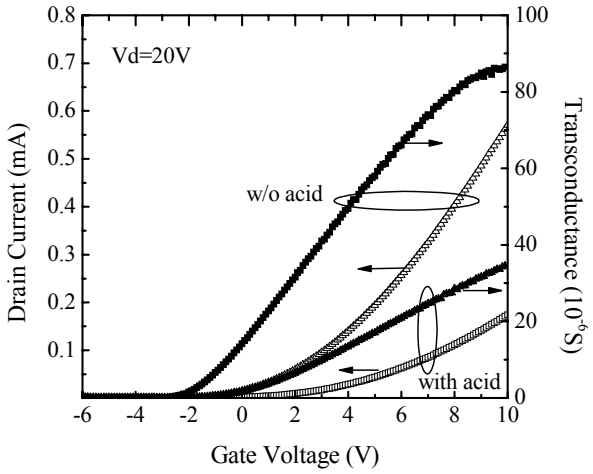

Fig. 4 The currents and transconductances of devices with or without acid treatment.

4. Mobility Measurement

To investigate the electron transport property in the channel, the devices measured above were used to measure the field-effect mobility. The field-effect mobility can be calculated as follows:

$$\mu_{FE} = \frac{G_M(V_g)}{C_G(V_g)}\frac{L^2}{V_D} \qquad (1)$$

Here, L is gate length, C_G is gate capacitance and G_M is transconductance in linear region, for instance, under drain voltage of 0.1 V. Gate capacitance was measured at 1 MHz and G_M was measured at 20Hz [4].

In a conventional method to measure field-effect mobility, the gate capacitance and the transconductance will be measured separately. In such case, it is possible that the interface states are in different conditions even at the same gate bias due to hysteresis effects. To avoid this problem, we made a measurement setup in which a relay was used to switch between the current measurement and the capacitance measurement under the same gate voltage supplied by HP 4284A impedance analyzer. The system is controlled by PC through GP-IB and VBA program.

The measured field-effect mobilities of the devices are shown in Fig. 6. The maximum field-effect mobility is around 65 cm^2/Vs. The mobility is still low and is considered to be due to the high density interface state and the quality of the structure.

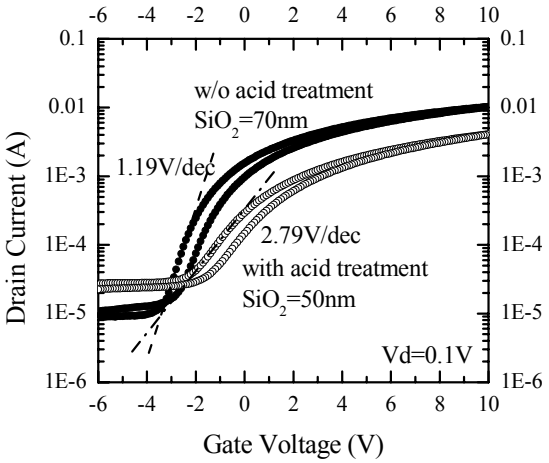

Fig. 5 Subthreshold characteristics for the MOSFETs.

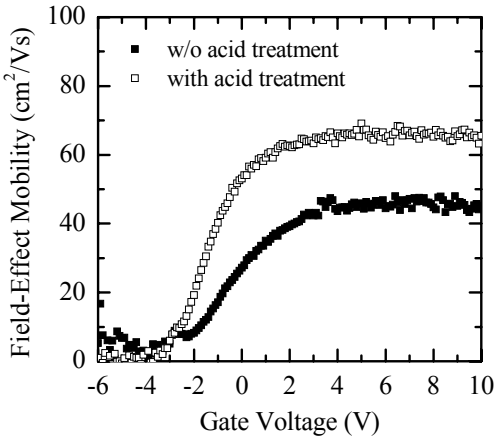

Fig. 6 The measured field-effect mobility of the device.

5. Conclusion

GaN MOSFETs with TEOS SiO_2 insulator was developed with AlGaN/GaN HFET structure as the source and drain regions. Operation up to gate voltage of 10 V was realized with low gate leakage current. A new method was developed to measure the mobility of a FET to avoid the affect from hysteresis. The maximum field-effect mobility is around 65 cm^2/Vs with interface state density of 9.3×10^{12}cm^2·eV .

References

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