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High-performance inversion-mode III-V MOSFETs enabled by atomic-layer-deposited high-k dielectrics (invited)

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1. Introduction

Using In-rich InGaAs as surface channel, high-performance inversion-type enhancement-mode high-k/III-V NMOSFETs have been demonstrated.[1-6] Although on-state performance, such as drain saturation current I_{dss} and peak transconductance g_m show promise, the off-state performance or subthreshold characteristics need to be seriously evaluated for potential applications in digital circuits. In this paper, we systematically study I_{dss}, g_m, threshold voltage (V_T), I_{on}/I_{off} ratio, sub-threshold swing (*S.S.*), the drain induced barrier lowing (*DIBL*), gate delay and energy delay product normalized to device width of the fabricated $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFETs, as function of the gate length from 110 nm to 250 nm.

2. Experiments and Results

Fig. 1 shows the schematic cross section of the device structure. The electron beam lithographically fabricated MOSFETs have 110 to 250 nm nominal channel lengths, L_{ch}, defined by the source-drain implant separation. The channel width of all measured devices is 5.0 µm. The detailed device fabrication flow is described in Ref. 7. The device process is not self-aligned. A well-behaved I-V characteristic of a 150 nm-gate-length is demonstrated in Fig. 2 and Fig. 3 with high drain current of 0.92 mA/µm and transconductance of 0.7 mS/µm for a surface channel III-V MOSFET.

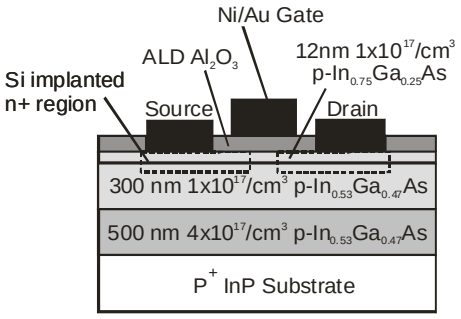

Fig.1 Schematic cross section of InGaAs NMOSFET with ALD Al_2O_3 gate dielectric.

Fig. 4 shows I_d and I_s in log scale vs. V_{gs} as a function of V_{ds} of the same device. It is clear that I_{sub} from the reverse-biased pn-junction leakage current determines the leakage floor and I_d at $V_{gs} < 0$ V at high V_{ds}. Junction leakage is significantly reduced by reducing the implanted source/drain activation temperature from 750 °C to 650 °C without sacrificing any on-state performance [1,2,7]. The gate leakage current through 5 nm Al_2O_3 is extremely low, at 10 pA/µm or 10^{-3}A/cm^2 level, about eight orders of magnitude lower than the drain current. Fig. 5 shows V_T reduction to lower voltage for shorter gate-length devices. The V_T is determined by the linear extrapolation method at V_{ds}=0.05V.

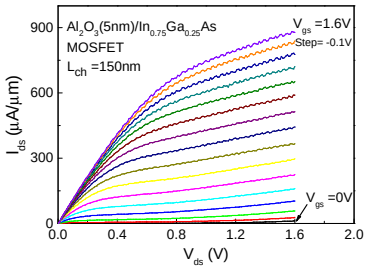

Fig.2 Drain current versus drain voltage at different gate biases for a 150 nm-gate-length MOSFET with a 5 nm ALD Al_2O_3 gate dielectric.

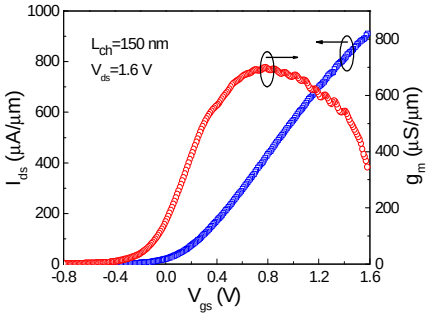

Fig.3 I_{ds} and g_m versus V_{gs} at V_{ds}=1.6V for the same $In_{0.75}Ga_{0.25}As$ MOSFET with L_{ch}=150 nm.

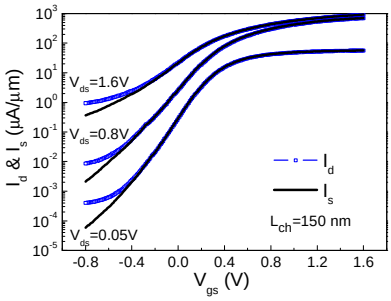

Fig.4 I_d and I_s at three different V_{ds} of the same $In_{0.75}Ga_{0.25}As$ MOSFET with L_{ch}=150nm.

Fig. 6 shows the subthreshold characteristics of drain current I_d vs V_{gs} for 4 representative devices with 110, 130, 160 and 200 nm gate lengths at V_{ds}=1.6 V and

V_{ds}=0.05 V. *SS* and *DIBL* are both derived from the semilog transfer characteristics of I_d at V_{ds}=0.05V and V_{ds}=1.6V. Large *SS* and *DIBL* are due to dominant donor traps at high-k/InGaAs interface with D_{it} of 2×10^{12}/cm^2-eV at CBM and even higher in the bandgap.[8] Table 1 summarizes the I_{dss}, g_m, *SS*, *DIBL*, I_{on}/I_{off} as functions of L_{ch} obtained from I_d. I_{on}/I_{off} is chosen as I_{on} (V_{ds}=1.6V, V_{gs}=1.2V)/ I_{off} (V_{ds}=1.6V, V_{gs}=-0.6V) or I_{on} (V_{ds}=0.05V, V_{gs}=1.2V)/ I_{off} (V_{ds}=0.05V, V_{gs}=-0.6V), which roughly agrees with 1μA/μm metric for V_T (V_T≈0 for 200 nm MOSFET at V_{ds}=1.6V) and 2/3 of gate swing above V_T to obtain I_{on} and 1/3 of the gate sweep below V_T to obtain I_{off}. It can be seen that *SS* and *DIBL* increase and I_{on}/I_{off} decreases with decreasing L_{ch}. The values start to deteriorate dramatically at L_{ch}=130 nm or shorter, indicating that severe short-channel effect occurs. Gate delay and energy gate delay product per width are also reported in Table 1. The numbers with gate length shorter than 130 nm are missing since the device is not well behaved. I_{on} values for L_{ch}≤130 nm have also not too much meaning since the device does not turn off well.

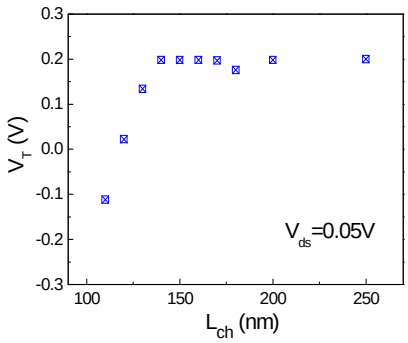

Fig.5 V_T vs. different L_{ch} from 110 nm to 250 nm. A clear roll-over effect is observed at L_{ch}≤130nm.

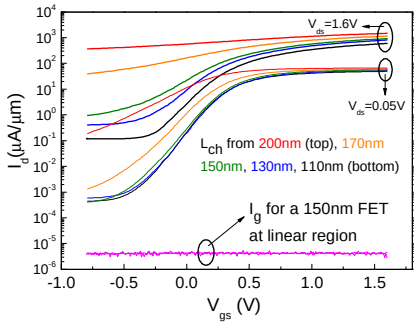

Fig.6 Subthreshold characteristics of 4 devices at V_{ds}=0.05V and V_{ds}=1.6V.

3. Conclusion

We have demonstrated deep submicron $In_{0.75}Ga_{0.25}As$ MOSFETs and systematically studied their on-state and off-state characteristics. Severe short-channel effects are observed at implanted surface channel devices with L_{ch}≤ 130 nm. Much more work on interface and junction, such as shallow junction engineering and halo implantation, are needed to make this novel device structure a competitive technology for deeply scaled CMOS technology nodes.

Table 1 Major device parameters of $In_{0.75}Ga_{0.25}As$ MOSFETs

L_{ch} (nm)	I_{on} (μA/μm) (V_{ds}=1.6V)	g_m (μS/μm) (V_{ds}=1.6V)	SS (mV/dec) (V_{ds}=0.05V)	SS (mV/dec) (V_{ds}=1.6V)	DIBL (mV/V)	I_{on} / I_{off} (V_{ds}=0.05V) V_{gs}=1.2V/ V_{gs}=-0.6V	I_{on} / I_{off} (V_{ds}=1.6V) V_{gs}=1.2V/ V_{gs}=-0.6V	Gate Delay (ps) (V_{ds} = 1.6V)	Energy Delay Product per Width (Js/μm) (V_{ds}=1.6V)
110	1485	750	430			150			
120	1333	760	291			1.0×10^3			
130	1160	760	222	1164	837	1.7×10^4	18	2.0	7.1×10^{-26}
140	1002	752	178	507	401	6.2×10^4	139	2.4	9.5×10^{-26}
150	925	700	169	355	283	8.3×10^4	526	2.8	1.2×10^{-25}
160	802	645	168	284	245	6.4×10^4	545	3.5	1.6×10^{-25}
170	800	632	167	250	210	7.0×10^4	605	3.7	1.8×10^{-25}
180	745	608	155	231	164	5.8×10^4	610	4.2	2.1×10^{-25}
200	740	584	154	213	157	8.7×10^4	659	4.7	2.6×10^{-25}
250	687	510	153	201	137	8.6×10^4	903	6.4	4.4×10^{-25}

Acknowledgment

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