High-performance inversion-mode III-V MOSFETs enabled by atomic-layer-deposited high-k dielectrics (invited)

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1. Introduction
Using In-rich InGaAs as surface channel, high-performance inversion-type enhancement-mode high-k/III-V NMOSFETs have been demonstrated. 
Although on-state performance, such as drain saturation current $I_{ds}$ and peak transconductance $g_m$ show promise, the off-state performance or subthreshold characteristics need to be seriously evaluated for potential applications in digital circuits. In this paper, we systematically study $I_{ds}$, $g_m$ threshold voltage ($V_T$), $I_{on}/I_{off}$ ratio, sub-threshold swing (S.S.), the drain induced barrier lowering (DIBL), gate delay and energy delay product normalized to device width of the fabricated Al$_2$O$_3$/In$_{0.75}$Ga$_{0.25}$As MOSFETs, as function of the gate length from 110 nm to 250 nm.

2. Experiments and Results
Fig. 1 shows the schematic cross section of the device structure. The electron beam lithographically fabricated MOSFETs have 110 to 250 nm nominal channel lengths, $L_{ch}$, defined by the source-drain implant separation. The channel width of all measured devices is 5.0 µm. The detailed device fabrication flow is described in Ref. 7. The device process is not self-aligned. A well-behaved I-V characteristic of a 150 nm-gate-length is demonstrated in Fig. 2 and Fig. 3 with high drain current of 0.92 mA/µm and transconductance of 0.7 mS/µm for a surface channel III-V MOSFET.

Fig. 4 shows $I_d$ and $I_s$, in log scale vs. $V_{gs}$, as a function of $V_{ds}$, of the same device. It is clear that $I_{sub}$ from the reverse-biased pn-junction leakage current determines the leakage floor and $I_d$ at $V_{gs} < 0$ V at high $V_{ds}$. Junction leakage is significantly reduced by reducing the implanted source/drain activation temperature from 750 °C to 650 °C without sacrificing any on-state performance [1,2,7]. The gate leakage current through 5 nm Al$_2$O$_3$ is extremely low, at 10 pA/µm or $10^{-2}$A/cm$^2$ level, about eight orders of magnitude lower than the drain current. Fig. 5 shows $V_T$ reduction to lower voltage for shorter gate-length devices. The $V_T$ is determined by the linear extrapolation method at $V_{ds} = 0.05$V.

Fig.2 Drain current versus drain voltage at different gate biases for a 150 nm-gate-length MOSFET with a 5 nm ALD Al$_2$O$_3$ gate dielectric.

Fig.3 $I_{on}$ and $g_m$ versus $V_{gs}$ at $V_{ds} = 1.6$V for the same In$_{0.75}$Ga$_{0.25}$As MOSFET with $L_{ch} = 150$ nm.

Fig.4 $I_d$ and $I_s$ at three different $V_{ds}$, of the same In$_{0.75}$Ga$_{0.25}$As MOSFET with $L_{ch} = 150$nm.

Fig. 6 shows the subthreshold characteristics of drain current $I_d$ vs $V_{gs}$ for 4 representative devices with 110, 130, 160 and 200 nm gate lengths at $V_{ds} = 1.6$ V and...
$V_{ds}=0.05$ V. $SS$ and $DIBL$ are both derived from the semilog transfer characteristics of $I_d$ at $V_{ds}=0.05$V and $V_{ds}=1.6$V. Large $SS$ and $DIBL$ are due to dominant donor traps at high-k/InGaAs interface with $D_{it}$ of $2\times10^{12}/\text{cm}^2\cdot\text{eV}$ at CBM and even higher in the bandgap. Table 1 summarizes the $I_{on}$, $g_m$, $SS$, $DIBL$, $I_{on}/I_{off}$ as functions of $L_{ch}$ obtained from $I_d$ at $V_{ds}=0.05$V or $V_{ds}=1.6$V, which roughly agrees with $1\mu\text{A}/\mu\text{m}$ metric for $V_T$ ($V_T \approx 0$ for 200 nm MOSFET at $V_{ds}=1.6$V) and 2/3 of gate swing above $V_T$ to obtain $I_{on}$ and 1/3 of the gate sweep below $V_T$ to obtain $I_{off}$. It can be seen that $SS$ and $DIBL$ increase and $I_{on}/I_{off}$ decreases with decreasing $L_{ch}$. The values start to deteriorate dramatically at $L_{ch}=130$ nm or shorter, indicating that severe short-channel effect occurs. Gate delay and energy gate delay product per width are also reported in Table 1. The numbers with gate length shorter than 130 nm are missing since the device is not well behaved. $I_{on}$ values for $L_{ch} \leq 130$ nm have also not too much meaning since the device does not turn off well. as shallow junction engineering and halo implantation, are needed to make this novel device structure a competitive technology for deeply scaled CMOS technology nodes.

3. Conclusion

We have demonstrated deep submicron In$_{0.75}$Ga$_{0.25}$As MOSFETs and systematically studied their on-state and off-state characteristics. Severe short-channel effects are observed at implanted surface channel devices with $L_{ch} \leq 130$ nm. Much more work on interface and junction, such

### Acknowledgment

The work is supported by National Science Foundation and SRC FCRP MSD Center. The authors thank D.A. Antoniadis for the valuable discussions.

### References