Fabrication of InP/InGaAs Undoped Channel MOSFET with Selectively Regrown N⁺-InGaAs Source Region

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1. Introduction

According to ITRS 2007 [1], III-V semiconductor device technology will potentially be combined with the LSI technology to realize circuits with capabilities that are greater than those of current CMOS circuits. In fact, logic applications using III-V devices have already been researched. In previous studies, conventional InP-based transistors were fabricated with HEMT device structures [2], [3]. Furthermore, high-k dielectric MOSFETs with III-V channels have been studied [4]. The ITRS stated that in future, MOSFETs will be expected to have a saturation drain current (\(I_d\)) that is as high as 3 A/mm. To fulfill this requirement using a III-V channel, the source doping concentration must be greater than \(1 \times 10^{19} \text{ cm}^{-3}\) [5]. However, in the case of III-V materials, it is difficult to obtain a high source doping concentration using ion implantation techniques. One of the solutions to this problem is to use MOSFETs with regrown source and drain (S/D) structures so that the transconductance (\(g_m\)) and saturation drain current (\(I_d\)) are enhanced; such MOSFETs can be used to realize high-speed and low-power-consumption devices [6]. The objective of our study is to fabricate MOVPE using a regrown source fabrication process, because this process allows the high penetration of lateral growth to fill the undercut.

Previously, we had demonstrated the selectively lateral growth of MOVPE in order to fill the undercut and fabricate a contact with a quantum well channel and regrown S/D [7] and MOSFET characteristics using a regrown source [8]. In this study, we introduced a highly doped regrown source in order to improve carrier injection and reduce the access resistance and undoped channel to suppress the ionized impurity scattering.

2. Device structure and fabrication process

Figure 1 shows the schematic of the MOSFET fabricated in this study. Its gate length \(L_g\) is 6 \(\mu\)m and its gate width \(W_g\) is 20 \(\mu\)m in design. The thickness of the InGaAs quantum well channel layer is 12 nm. The InGaAs was covered by a 5-nm-thick InP layer to improve the interface condition. The MOSFET fabrication process is described as follows. First, \(\text{SiO}_2\) dummy gate structures were fabricated by plasma enhanced (PE) CVD and \(\text{CF}_4\) dry etching using an Al mask for selective regrowth. Second, an undercut into InGaAs channel was formed using citric acid:\(\text{H}_2\text{O}_2\) = 1:1 solution, and InAlAs surface treatment was carried out when the ratio of the concentrations of HCl:\(\text{H}_2\text{O}\) = 1:5. Then, samples were immediately loaded into an MOVPE chamber.

After regrowth, device isolation was carried out using citric acid solution. Next, the dummy gates were removed using BHF and replaced with a 20-nm-thick gate insulator by PECVD (Fig. 2) with InP surface passivation using \((\text{NH}_4)_2\text{S}\) solution. Then, Al/Au gate electrodes were formed by vacuum deposition. S/D contact holes are etched using BHF. Finally, Ti/Pd/Au S/D electrodes were deposited by electron beam deposition.

As shown in Fig. 2, the SEM image indicates that a regrown InGaAs source region was formed without void formation at the boundary with a channel. The buried length was approximately 40 nm.

To evaluate the effect of S/D doping density and channel doping density, three different MOSFETs were fabricated. First, a MOSFET with an n-doped \((1 \times 10^{18} \text{ cm}^{-3})\) channel and low doped S/D was fabricated. Second, The S/D doping density was increased to reduce the access resistance. Finally, an undoped channel device with n⁺-S/D was fabricated to increase the driving current.
3. I-V characteristics of the fabricated MOSFETs

From the I–V measurement of the n-doped channel device structure with low-doped (which was clarified by post Hall measurement as follows) S/D, $I_d$ (at $V_g = 3$ V and $V_d = 2$ V) was 175 mA/mm and the maximum transconductance ($g_m$) was 9.0 mS/mm at $V_d = 0.5$ V. The effective carrier mobility was estimated from the maximum extrinsic $g_m$, the gate capacitance $C_{ox}$ (as SiO$_2$ insulator capacitance) and $V_d = 0.5$ V using a long channel device model ($I_d = \mu_{eff}C_{ox}(V_g - V_{th})V_dW_g/L_g$). It was approximately 625 cm$^2$/Vs. The $g_m$ and mobility were lower than the expected values. The major reason for this result was the S/D access resistance. In the Hall measurement, carrier density of the regrown S/D was below $1 \times 10^{19}$ cm$^{-3}$, which was one tenth the required value.

Therefore, the flow rate of Si$_2$H$_6$ in MOVPE regrowth was increased by a factor of 6. The carrier density of regrown InGaAs was increased to $1.15 \times 10^{19}$ cm$^{-3}$. Then, $g_m$ and the effective mobility were also increased to 30.3 mS/mm and 2106 cm$^2$/Vs, respectively. These values were over 3 times higher than those of the MOSFET with a low-doped S/D device. This was because of a reduction in the S/D access resistance.

Under the same MOVPE growth condition for highly doped S/D, an undoped channel MOSFET was fabricated in order to reduce the ionized impurity scattering and enhance the effective mobility. In the measurement of the undoped channel MOSFET (Fig. 3 (a)), current saturation was clearly observed and $I_d$ (at $V_g = 3$ V and $V_d = 2$ V), and it was approximately 434 mA/mm. The measured $g_m$ was 43.6 mS/mm at $V_d = 0.5$ V (Fig. 3 (b)). This value was around 1.5 times greater than that of the n-doped channel MOSFET with similar n$^+$-S/D. The extrinsic effective mobility, which was estimated from these parameters, was 3030 cm$^2$/Vs.

In spite of using an undoped channel, the threshold voltage $V_{th}$ was still low ($\sim -2$ V, equivalent to that of the n-type channel), and an enhancement mode operation was not obtained. This phenomenon can be explained by the existence of interface traps between SiO$_2$ and InP. Hysteresis in $I_d$–$V_g$ measurement also suggests the existence of interface states. To control $V_{th}$, materials used to fabricate gate stack structures (insulator and metal) and surface treatment technology of InP or InGaAs need to be optimized.

In future, a doping density higher than that of the current S/D will be required in order to improve electron injection and reduce the access resistance. Moreover, a detailed evaluation of carrier density and effective mobility will be required, such as split C-V method to improve channel design.

5. Conclusions

We fabricated an undoped InP 5 nm/InGaAs 12 nm composite channel MOSFET using MOVPE regrown source and drain structures. The maximum $g_m$ was 43.6 mS/mm at $V_d = 0.5$ V and the effective mobility roughly estimated from $g_m$ was 3030 cm$^2$/Vs. The mobility was 4.8 times larger than that of a doped channel device with a low-doped regrown source. This was probably attributed to a reduction in the access resistance and ionized carrier scattering.

![Fig. 3 I–V characteristics of undoped channel MOSFET with highly doped regrown source](image)

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**References**