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Heteroepitaxy of Si_xGe_{1-x} (x < 5%) source/drain on GaAs substrates for the application of III-V MOSFETs

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Introduction

With Si CMOS technology scaling into 22nm node or beyond, various high-mobility III-V materials, like (In)GaAs and InSb, have been widely investigated as the n-channel candidates with high-*k* gate dielectrics [1]-[2]. However, III-V materials, in general, possess the lower values of n-type dopant solubility and the density of states, possibly becoming the bottlenecks in outperforming the nano-scale Si devices. For GaAs, the values of DOS and the maximum Si solubility are only 4.7×10^{17} and 1×10^{19} cm^{-3}, respectively, which are two and one orders of magnitude lower than those in Si. Hence, we proposed a new structure of GaAs MOSFET having SiGe source/drain (S/D) to tackle these critical problems and boost the current drive capability. Moreover, SiGe S/D also facilitates the integration of silicide/germanide technologies in the proposed III-V heterojunction devices.

2. Experimental

Diode structures were fabricated on p-GaAs(100) substrates. Subsequently, a 400-nm-thick SiO_2 layer was deposited by using PECVD and then S/D region was recessed by etching SiO_2 and GaAs in the BOE and diluted H_2SO_4 acid solutions, respectively. Prior to selective growth of Si_xGe_{1-x} in UHVCVD, the patterned GaAs samples were soaked in the diluted HCl solution for 2 min, followed by thermal desorption at 500 °C for 10 min. We grew a series of Si_xGe_{1-x} (x < 5%) films by adjusting the flow ratio of GeH_4 and SiH_4 precursors, where the temperature and pressure were kept at 500 °C and 30 mTorr, respectively. The surface morphology and epitaxial quality of SiGe films were characterized by AFM and TEM, while the composition was examined by XRD. In order to fabricate the heterojunction diodes, P dopant was implanted (1×10^{15} /cm^2, 30 keV) into Ge and activated at 600 and 700 °C for 30 s in N_2 ambient with SiO_2 capping. After excavating the S/D contact holes, Al and Au/Ni/Au were deposited as the top and backside contacts, respectively.

3. Results and Discussion

Figure 1 shows the TEM images of the Ge heteroepitaxy on GaAs S/D region. Almost lattice-matched Ge films were successively grown, in which the thickness was ca. 710 nm for the time of 45 min, but, there were somewhat surface impurities existed at the interface. Fig. 2 plots the variation of Ge thickness versus the growth time. The growth was the island mode at the initial stage (< 30 min) with the slower rate; after that, it entered into the blanket mode with the accelerated rate, implying the existence of growth incubation time (T_{inc}) during Ge/GaAs heteroepitaxy. We suggest that surface stoichiometry of GaAs was strongly dependent on the wet cleaning steps, and the temperatures and pressures employed in surface desorption and film growth, which in turn determines the resultant T_{inc}. Furthermore, as shown in Figs. 3(a)-(d), we also achieved the epitaxy of almost dislocation-free and crystalline $Si_{0.03}Ge_{0.97}$ and $Si_{0.05}Ge_{0.95}$ films on GaAs, in which the thicknesses were ca. 383 and 185 nm for times of 70 and 50 min, respectively. It indicates that the epitaxy of SiGe on GaAs has a relatively longer T_{inc} than that of Ge on it. From the XRD spectra (Fig. 4), the Ge and SiGe (004) diffraction peaks were clearly observed in these samples, however, without observation of their interference fringes. The values of full width at half maximum were 0.02, 0.028, and 0.037 degree for the Ge, $Si_{0.03}Ge_{0.97}$ and $Si_{0.05}Ge_{0.95}$ films, indicative of the Si_xGe_{1-x} crystallinity deterioration with increasing the degree of the lattice mismatch. In Fig. 5, the AFM analysis revealed that the roughness gradually reduced with increasing the epitaxial thickness; interestingly, SiGe seemed to have the flatter surface morphology with respect to Ge. The possible mechanism is that addition of the Si atoms makes the bonding probability of Ge and Ga atoms become slower, in consequence, the roughness induced mainly by self accumulation of As atoms also becomes relievable. Figs. 6 and 7 demonstrate the I-V and breakdown characteristics of the n^+-Ge/p-GaAs heterojunctions. The 600°C-annealed diode, relative to 700°C-annealed one, exhibited a higher forward current J_F (~9.5×10^1 A/cm^2) and a lower reverse current J_R (~7.7×10^{-3} A/cm^2), in which the rectifying ratio of ca. 10^4 within ± 1 V. Here, the J_R curves revealed a somewhat exponential V_R-dependent behavior also with the higher temperature sensitivity, implying the dominance of the trap-assisted tunneling mechanism in these diodes; such behavior was relieved with receiving higher activation temperature of 700 °C. The breakdown voltages of the 700°C-annealed diode ranged from 14 to 17 V at 20 °C and decreased to the range 10-12 V at 100 °C.

4. Conclusions

We demonstrated the GaAs heterostructure with the embedded Si_xGe_{1-x} (x < 5%) S/D. It is expected that this novel structure possesses higher electron mobility and thermal velocity in the channel and also has higher DOS value and dopant level in S/D for MOSFET operation. Moreover, Si_xGe_{1-x} S/D was believed to provide the tensile strain within the GaAs n-channel, assisting to enhance the

driving current further. We manifested the feasibility of MOSFET application by fabricating the n^+-Ge/p-GaAs heterojunction, which showed the rectifying ratio of 10^4 after undertaking lower thermal budget (600 °C).

References

[1] H.-C. Chin *et al.*, *IEDM*, p. 383, 2008.

[2] M. Radosavljevic *et al.*, *IEDM*, p. 727, 2008.

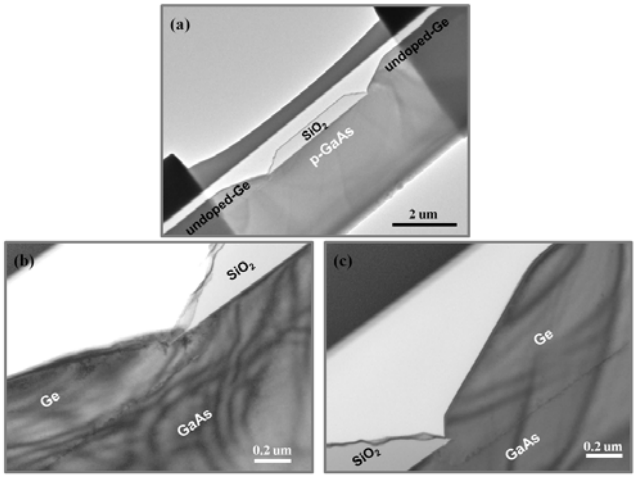

Fig. 1. The TEM images of selective Ge heteroepitaxy on the recessed GaAs S/D region.

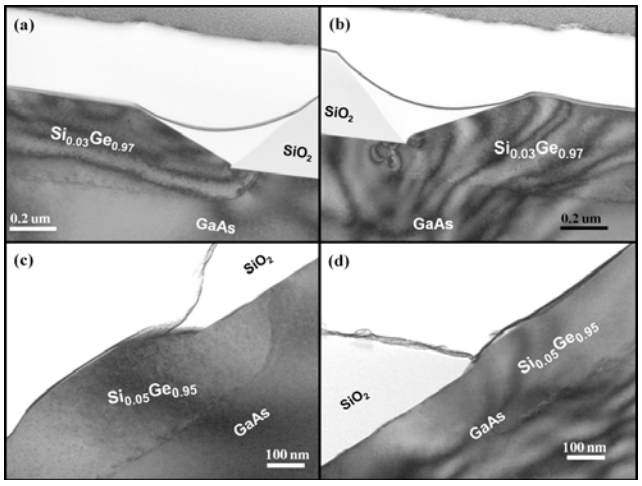

Fig. 3. The TEM images of selective Si_xGe_{1-x} heteroepitaxy on recessed GaAs S/D region: (a)-(b) $Si_{0.03}Ge_{0.97}$ film and (c)-(d) $Si_{0.05}Ge_{0.95}$ film.

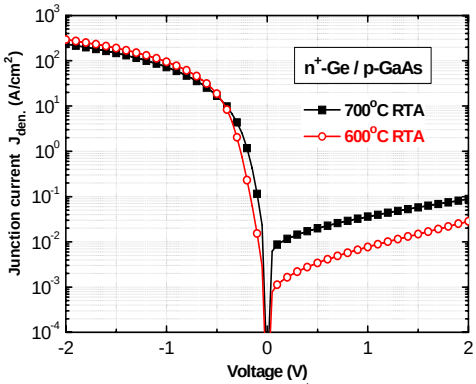

Fig. 6. The diode characteristics of n^+-Ge/p-GaAs heterojunctions undertaking 600 and 700 °C activation for 30 s with SiO_2 capping.

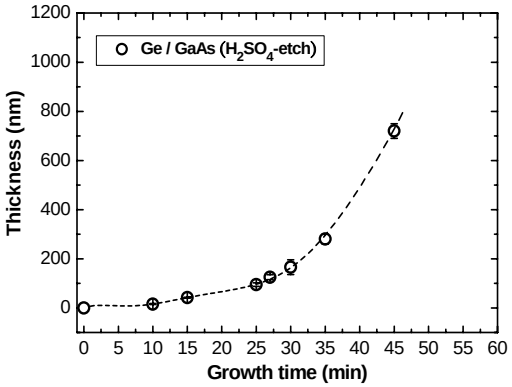

Fig. 2. The thickness of Ge film on the recessed GaAs substrate as a function of the growth time.

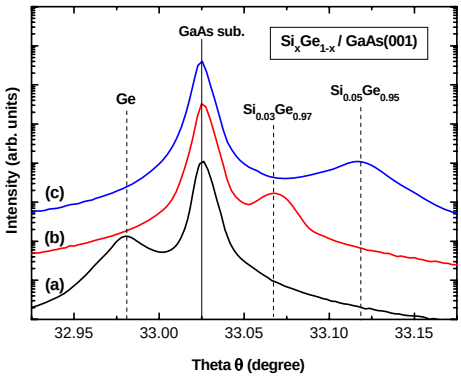

Fig. 4. The XRD curves of Ge, $Si_{0.03}Ge_{0.97}$ and $Si_{0.05}Ge_{0.95}$ films on the patterned Ga As substrate.

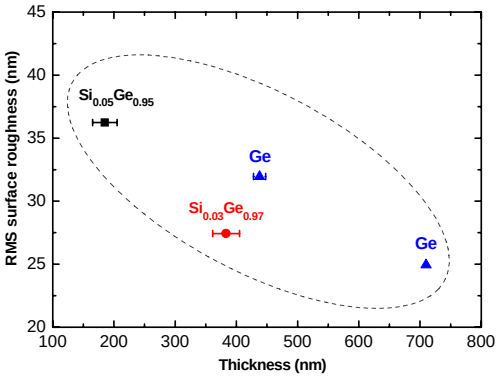

Fig. 5. The AFM root-mean-square (RMS) roughness of Ge, $Si_{0.03}Ge_{0.97}$, and $Si_{0.05}Ge_{0.95}$ films versus the epitaxy thickness.

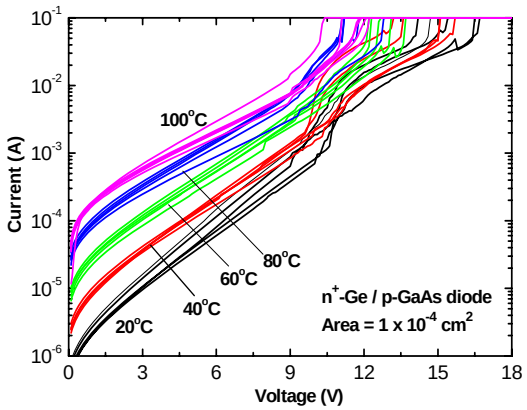

Fig. 7. Temperature dependent J_R curves of n^+-Ge/p-GaAs heterojunction with 700 °C dopant activation for 30s.