Metalorganic vapor phase epitaxy of GaAs with AlP surface passivation layer for improved MOS characteristics

Yuki Terada[1,*], Momoko Deura[1] , Yukihiro Shimogaki[2], Yoshiaki Nakano[1,3], and Masakazu Sugiyama[1,4]

[1]Univ. of Tokyo, Dept. of Electrical Engineering and Information systems, School of Engineering
2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6753　E-mail: yuki@hotaka.t.u-tokyo.ac.jp
[2]Univ. of Tokyo, Dept. of Materials Eng., School of Engineering
[3] Univ. of Tokyo, Research Center for Advanced Science and Technology
[4]Univ. of Tokyo, Institute of Engineering Innovation, School of Engineering

1. Introduction

Suppression of interface state density is the essence of the improved performance III-V MOS transistor, which is promising for the high-speed and low-power operation by using high electron mobility (In)GaAs as a channel layer. Since arsenic oxide (As oxide) is well known as one of the origins of interface states, suppression of surface oxidation is a quite important issue [1], although it is usually inevitable upon air exposure of the surface.

In order to provide the surface of a III-V epitaxial layer with anti-oxidation function, we have investigated the *in situ* surface passivation using Al in a metalorganic vapor phase epitaxy (MOVPE) reactor [2]. In this method, a thin Al layer is formed by the supply of Al source, trimethylaluminum (TMA), subsequent to the growth of a III-V layer. This Al layer is usually oxidized to Al_2O_3 and protects the underlying III-V layer from oxidation, serving as a surface passivation layer. Since Al_2O_3 is a common gate dielectric, we can obtain the Al_2O_3/III-V gate stack structure without any interlayer by the deposition of the Al_2O_3 on the passivation layer. **Figure 1** shows a schematic of a series of III-V MOS process using the *in situ* surface passivation proposed here.

We have examined the effect of such in situ passivation by MOVPE using GaAs as a standard III-V layer because it has been the target of the most intensive research. The Al passivation layer successfully suppressed the formation of As oxide upon air exposure. When we examined the effect the Al passivation layer on the C-V characteristics of GaAs MOS structure, however, we found that the morphology of the passivation layer was rough, resulting in poor C-V characteristics.

Therefore, in this study, we focused on a thin AlP (aluminum phosphide) passivation layer. Unlike the deposition of the thin Al layer, we can expect an AlP layer with extremely smooth surface due to the coexistence of the group-V precursor (tertiarybutylphosphisne, TBP) in the growth process. It is also expected that the AlP layer converts to Al_2O_3 by oxidation, similarly to the case of the Al passivation layer. Similar function is expected for a thin AlAs layer grown on GaAs, but oxidation of AlAs yields As oxide on the surface of GaAs, which is definitely not allowable for MOS structures. In order for the AlP

passivation layer to be effective, therefore, it is mandatory that no As contamination exists in the AlP layer.

Arsenic-free AlP layer can only be grown on the GaAs if we purge As completely from the GaAs surface prior to the growth of AlP. The amount of excess surface As can be estimated in terms of surface reconstruction of the GaAs surface, which we can observe *in situ* in the course of the growth. In this study, we were able to obtain c(8×2) surface reconstruction that has the lowest As content that we have ever observed. The heart of the effective As purge from the surface is the supply of H_2S after the growth of GaAs. It is expected that residual As atoms are exchanged by the adsorption of sulfur atoms. The adsorbed sulfur atoms are easily desorbed by successive H_2 annealing [3], resulting in the low-As-content c(8×2) surface.

Such sophisticated growth sequence allowed us to grow the AlP layer without As contamination. The layer prevented generation of As oxide as we expected as well as it converted to Al_2O_3 upon air exposure. We further optimized its growth process to achieve high-performance GaAs MOS structure.
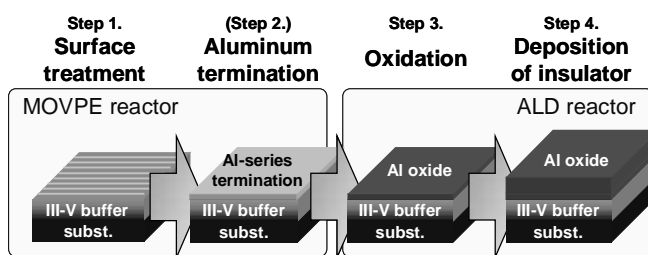

Fig. 1　Schematic of III-V MOS process using the *in situ* surface passivation with Al(P) in a MOVPE reactor.

2. Experimental setup

We used a horizontal single-wafer MOVPE reactor with a commercial RAS (Reflectance Anisotropy Spectroscopy) system for *in situ* observation of surface reconstructions during growth. Growth was performed at the total pressure of 10 kPa with H_2 as the carrier gas at 600℃. Group-III source materials were TMGa (Trimathylgallium) and TMAl while group-V sources were TBAs (Tertiarybutylarsine) and TBP. A 500-nm-thick n-GaAs ($5×10^{-17}$ cm^{-3}) layer was grown on a n-GaAs (001) substrate, fol-

lowed by the growth of AlP passivation layer with the thickness of roughly 0.3nm. After the growth, the surfaces was exposed to air and analyzed by XPS. The 6-nm-thick Al_2O_3 gate dielectric was deposited on the AlP-passivated surface by atomic layer deposition (ALD) for C-V measurement. Both of the gate metal and the contact of the substrate were Ti/Au.

3. Results and discussion

First, we optimized the gas-switching sequence between the growth of GaAs and AlP. As shown in **Fig. 2**, during the H_2 annealing after the growth of GaAs, the surface reconstruction converts from As-rich c(4×4) to less As-rich (2×4). Further reduction of surface As, that is, conversion to c(8×2) reconstruction was achieved by the flow of H_2S and succeeding H_2 annealing. We can identify these surface reconstructions in terms of the RAS by comparing the observed spectra with the ones in the literatures [4, 5]. By the use of *in situ* RAS, we can observe transition among those surface reconstructions and can exactly determine the period of each gas-supply step.
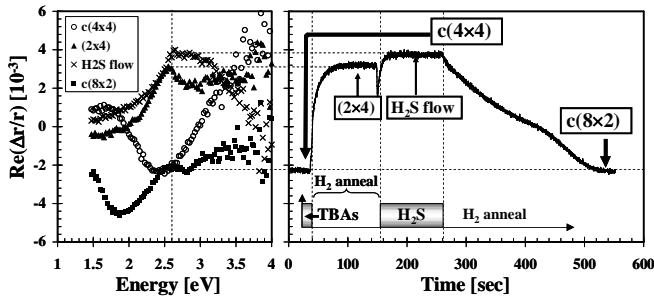

Fig. 2 [Left] The reflectance anisotropy (RA) spectra of surface reconstructions, corresponding to the RA value in the right figure.
[Right] The transient RA signal at the photon energy of 2.6eV during the surface treatment.

Next, we optimized the growth condition of the AlP passivation layer. Firstly, we focused on the growth temperature. **Figure 3** shows the As 3d XPS peak observed after air-exposure for the samples with the AlP passivation layer grown at different temperatures on c(8×2) GaAs surface. While the samples with the growth temperature of 650°C and 600°C show a slight As oxide peak, the sample with the AlP grown at 550°C was completely free from As oxide peak. This result indicates that the AlP passivation layer with the low growth temperature is appropriate as the passivation layer. The Al 2p XPS peak for 550°C indicates that the AlP converted Al_2O_3 upon air exposure as we expected.

Photoluminescence (PL) measurement confirmed that the low growth temperature of AlP is effective to suppress the interface states. PL intensity is a convenient measure of interfacial states because they act as nonradiative recombination centers. As shown in **Fig. 4**, PL intensity increases as the growth temperature of AlP decreases, indicating better surface passivation effect of AlP grown at 550°C.

Smoothness of the surface of the passivation layer seems to be the final critical factor to determine the C-V characteristics of a MOS structure. **Fig. 4** also shows AFM images of the surface of AlP passivation layers with the growth temperatures of 550°C and 650°C. The AlP layer grown at 550°C, which showed better anti-oxidation performance and led to the improved PL intensity, indeed exhibited smaller RMS, i.e., smoother surface. Further improvement on the RMS was achieved by increasing the TMAl partial pressure and reducing the growth period proportionally. As a result, the passivation layer with extremely smooth surface (RMS = 0.18nm) was obtained. This AlP layer is quite promising to exhibit excellent C-V characteristics.
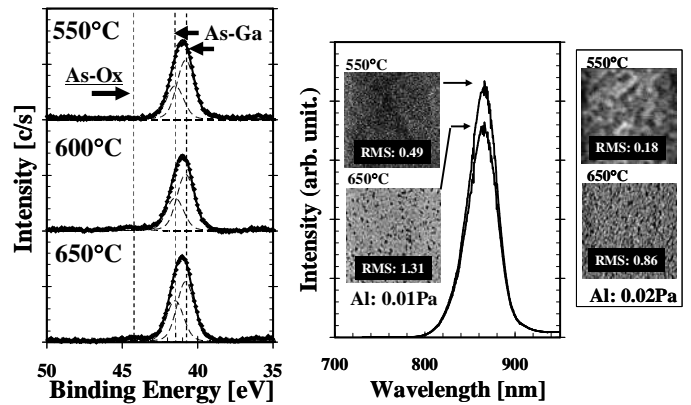

Fig. 3   As3d XPS spectra of the AlP passivated samples with the growth temperature of 550C, 600C, and 650C.

Fig. 4   PL spectra of the samples with the growth temperature of 550°C and 650°C (Al pressure of 0.01Pa), and AFM images of the sample with the Al pressure of 0.01 Pa and 0.02 Pa.

4. Conclusions

In order to realize a high-performance III-V MOS structure, we proposed novel method of AlP passivation accompanied by the H_2S flow for obtaining low-As-content c(8×2) surface between the growth of GaAs and AlP. We confirmed the complete suppression of As oxide, smooth morphology, and increased PL intensity by optimizing the growth condition of AlP. Electric property of GaAs MOS structure using the AlP passivation and H_2S treatment is quite promising.

References

[1] L. G. Meiners and H. H. Wieder; Mater. Sci. Rep. **3** (1988) 139
[2] Y. Terada, M. Deura, Y. Shimogaki, M. Sugiyama, Y. Nakano; J. Cryst. Growth **310** (2008) 4808
[3] D. Paget, J. E. Bonnet, V. L. Berkovits, P. Chiaradia, J. Avila; Phys. Rev. **B53** (1996) 4604
[4] A. Ohtake; Surf. Sci. Rep. **63** (2008) 295
[5] I. Kamiya, D. E. Aspnes, L. T. Florez, J. P. Harbison; Phys. Rev. **B46** (1992) 15894