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$In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$ Barrier Enhancement-mode Pseudo-morphic High Electron Mobility Transistor with an Enhanced Gate Forward Turn-on Voltage

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1. Introduction

Enhancement-mode pseudomorphic High Electron Mobility Transistors (E-pHEMTs) were thought to be promising for wireless handset applications because of high efficiency, low voltage single supply operation and no need for drain switch [1]. But E-pHEMTs had a poor threshold voltage (V_{TH}) controllability, a reliability issue and a low drain current density.

The low drain current density of E-pHEMTs is problematic in two aspects. The first is in a fabrication cost. E-pHEMTs occupy a larger chip size than depletion-mode pHEMTs (D-pHEMTs) or HBTs to meet current density requirements for applications. The second is in a gate Schottky reliability and its operating gate current. E-pHEMTs with an inferior drain current density need a higher V_{GS} to meet drain current requirements and increasing the V_{GS} accompanies a higher gate current. Operating current densities of GaAs Schottky diodes were thought to impact the long term reliability of the diodes [2].

Thus there have been many efforts to decrease the gate current and to increase the operating gate voltage. Glass *et al*. adopted a wide band-gap barrier layer for its large conduction band discontinuity (ΔE_C) [3]. Superlattice-insulated -gate field effect transistors (SIGFETs) adopted alternating thin layers of wide band-gap layer and narrow band-gap layer [4]. The superlattice suppressed gate current and increased applicable gate bias range. Palacios *et al*. proposed an AlGaN/GaN HEMT with a GaN spacer between GaN channel and AlGaN barrier which reduced the alloy scattering of electrons with AlGaN barrier [5].

This paper presents a new layer structure for E-pHEMT adopting a narrow band-gap layer as a part of barrier layers, $In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$. The barrier layer contained the narrow band-gap material of $In_{0.22}GaAs$. The impacts of the $In_{0.22}GaAs$ layer on gate current and $I_{DS.MAX}$ were examined.

2. Layer structure and process

Fig. 1 shows layer structures employed in this study. Type I layer structure was a newly devised one and adopted $In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$ barrier layer. Type II is the same as the type I layer structure except for its barrier layers. Type II layer structure adopted $In_{0.49}GaP/Al_{0.45}GaAs/Al_{0.22}GaAs$ barrier layer for comparison [6].

For the type I structure the narrow band-gap layer of $In_{0.22}GaAs$ is inserted between the wide band-gap layer of $Al_{0.45}GaAs$ and the spacer layer of $Al_{0.22}GaAs$. Its impacts can be understood in three ways. The first is electron confinement in a potential well. Fig. 2(a) shows that the $In_{0.22}GaAs$ barrier layer forms a potential well and some of electrons in the barrier layers are confined in the potential well at V_{GS} of 1.1V. Forward biased gates attract the electrons in the potential well and the electrons face ΔE_C between $Al_{0.45}GaAs$ and $In_{0.22}GaAs$ and the ΔE_C is 0.51 eV [7][8]. In contrast the type II has the barrier layers of $Al_{0.45}GaAs/Al_{0.22}GaAs$ and ΔE_C is 0.16 eV. Electron confinement in the $In_{0.22}GaAs$ potential well and large ΔE_C between $Al_{0.45}GaAs$ and $In_{0.22}GaAs$ might hinder the vertical flow of electrons from channel to gate for the type I layer structure. The second is conduction band enhancement of $Al_{0.45}GaAs$ for type I layer structure. In fig. 2(a) the $Al_{0.45}GaAs$ of type I structure at $Al_{0.45}GaAs/In_{0.22}GaAs$ interface had 0.035 eV higher E_C than that of type II structure at $Al_{0.45}GaAs/Al_{0.22}GaAs$ interface. The enhancement of E_C is attributed to lower electron density in the $Al_{0.45}GaAs$ layers. The third is drainage of barrier electrons to drain electrode. Electrons in the barrier are attracted to gate and form gate current. Some of these electrons can be swept to a positively biased drain. The $In_{0.22}GaAs$ layer is directly connected to drain and this layer can promote the drainage of electrons to drain. This might decrease gate current.

Layer	Material	Thickness(Å)
Cap	n+ GaAs	400
Barrier	$In_{0.49}GaP$	30
	$Al_{0.45}GaAs$	60
	$In_{0.22}GaAs$ for type I ($Al_{0.22}GaAs$ for type II)	30
	δ-doping	
	$Al_{0.22}GaAs$	30
Channel	$In_{0.22}GaAs$	110
Barrier	$Al_{0.22}GaAs$	40
	δ-doping	
	$Al_{0.22}GaAs$	710
Buffer & Substrate		

Fig. 1. The layer structures of E-pHEMTs

The two layers grown in molecular beam epitaxy (MBE) had the electron mobility of 5000 $cm^2/V \cdot s$ and the channel carrier density of 1.2×10^{12} cm^{-2}. After MESA isolation using a phosphoric based wet etchant, the ohmic metal of Ni/Ge/Au/Ni/Ag/Au(100/450/1000/100/1000/1000 Å) was deposited and annealed at 440°C. 0.5 um T-gates were defined using electron-beam lithography. Gate recess

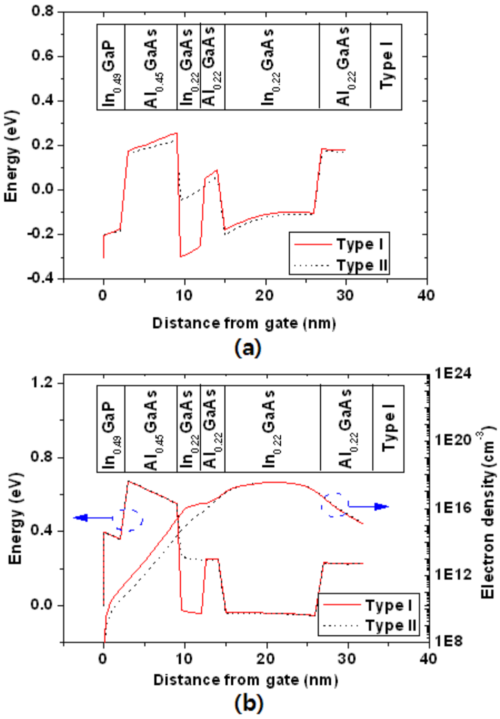

Fig.2. (a) The simulated conduction band diagram at the V_{GS} of 1.1 V, (b) the simulated conduction band diagram and the electron density at the V_{GS} of 0.4 V

was done using a selective phosphoric acid etchant (H_3PO_4:H_2O_2:H_2O=1:1:25) for 25 s. Pt/Ti/Pt/Au was deposited as a gate metal. And the final device was fully passivated using Si_3N_4 layer.

3. Measurement and discussions

The measured gate I-V curves in fig. 3 were in accordance with the simulations. At V_{GS} of 1.1 V the gate current density of the type I was lower than that of the type II by an order of magnitude. Gate forward turn-on voltage ($V_{G.ON}$) defined at the I_G of 1 mA/mm was 1.4 V for the type I and 1.1 V for the type II. From inset of the fig. 3 it can be noticed that the type I had a higher gate current at V_{GS} below 0.7 V. For this gate bias thermionic emission is not a dominant conduction mechanism for gate current and tunneling of electrons between the gate and the $In_{0.22}GaAs$ barrier layer might increase the gate current density. Fig. 2(b) shows the conduction band diagrams and the electron densities at V_{GS} of 0.4 V. Both structures had similar conduction band edges in the $Al_{0.45}GaAs$ layer. But the type I had a higher electron density in the $Al_{0.45}GaAs$ layer than the type II for tunneling of electrons. Off-state breakdown voltage (BV_{DG}) defined at the I_G of -1 mA/mm was about -7 V for both structures. They had rather small BV_{DG} values for single recessed gates.

Fig. 4 shows the transfer-curves and the measured maximum available gains (MAG) at V_{DS} of 1.5 V. They had the V_{TH} of 0.3 V at I_{DS} of 1 mA/mm. $I_{DS.MAX}$ was defined at the V_{GS} of $V_{G.ON}$ and the type I had a higher $I_{DS.MAX}$ for its enhanced $V_{G.ON}$. The $I_{DS.MAX}$ was 390 mA/mm for the type I and 275 mA/mm for the type II. $G_{M.MAX}$ was 450 mS/mm for the type I and 460 mS/mm for type II. The type

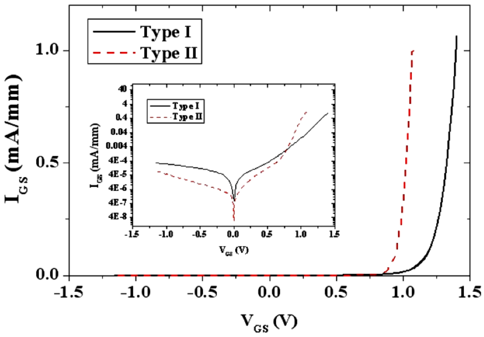

Fig.3. The measured gate Schottky IV curves

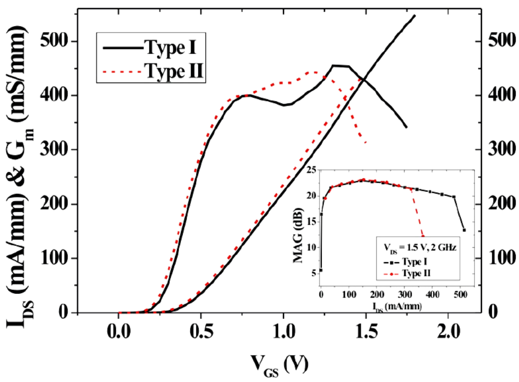

Fig.4. The measured transfer curves at the V_{DS} of 1.5 V and the MAG at the frequency of 2 GHz and the V_{DS} of 1.5 V

I didn't show a G_M degradation up to V_{GS} of 1.4 V while the type II showed a severe degradation at V_{GS} over 1.2. The MAG was measured at the frequency of 2 GHz and the V_{DS} of 1.5 V. The type I had a flat MAG for a wider range of I_{DS} than the type II.

4. Conclusions

A new E-pHEMT layer structure adopting the narrow band-gap layer as a barrier layer is reported. The barrier layer of $In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$ was more effective in enhancing the $V_{G.ON}$ than the barrier layer of $In_{0.49}GaP/Al_{0.45}GaAs/Al_{0.22}GaAs$. A larger V_{GS} bias could be applied to the $In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$ barrier E-pHEMT for its higher $V_{G.ON}$. The heterostructural concept of this work can be useful not only for the E-pHEMT but also other devices that need smaller gate leakage current.

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