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Extraction of Drain Current and Effective Mobility in Epitaxial Graphene Channel FETs on Silicon Substrates

Hyun-Chul Kang[1], Roman Olac-vaw[1†], Hiromi Karasawa[1], Yu Miyamoto[1], Hiroyuki Handa[1], Tetsuya Suemitsu[1,2], Hirokazu Fukidome[1,2], Maki Suemitsu[1,2], Taiichi Otsuji[1,2]

[1]Research Institute of Electrical Communication, Tohoku University
2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan
Phone: +81-022-217-6108, Fax: +81-022-217-6106, E-mail: kang@riec.tohoku.ac.jp
[2]JST-CREST, Japan Science and Technology Agency, Tokyo 107-0075, Japan

1. Introduction

Since the discovery in 2004, graphene, a single layer of graphite, has been a promising material for post-Si-CMOS devices due to its excellent carrier mobility [1,2]. Attempts to make graphene transistors have been reported [3]. The most popular method to obtain graphene samples is the manual exfoliation [1]. However, from the industrial adaptability point of view, epitaxial graphene (EG), which is produced by a thermal decomposition of SiC at high temperature in ultrahigh-vacuum (UHV) condition [4], is a more engineering way. Recently we have reported the first epitaxial graphene on Si substrates using high quality and appropriate crystal orientation of a thin SiC layer grown on a Si wafer [5]. In this work, we confirmed few-layer graphene (FLG) was successfully formed. The backgate-field-effect transistors using the epitaxial graphene on Si substrates were also demonstrated [6]. The SiC layer on the Si substrate was used as the insulating layer for the backgate transistors. In this paper, we study more exact current model for FLG FET and estimate the effective electron mobility in FLG channel. The drain current modulated by the gate voltage is clearly observed. The device exhibits behaviors of n-type transistors with the effective mobility exceeds the universal mobility of silicon.

2. Experimental

A schematic of the device's cross-section is shown in Fig. 1(left). The epitaxial graphene was formed on the surface of 3C-SiC(110) grown on a B-doped p-type Si(110) substrate. 3C-SiC was grown by gas-source molecular beam epitaxy (GSMBE) using monomethyl silane (MMS) at a pressure of 3.3×10^{-3} Pa [5]. The SiC growth process consists of two stages. First, a buffer-layer is formed (600℃ for 5 min) and a subsequent SiC growth (1000℃ for 120 min). For this growth condition, the thickness of the SiC layer is 80 nm. After that, the sample is annealed in vacuum at 1200℃ for 30 minutes to form a graphene film at the surface of SiC. The device process starts with the formation of ohmic contacts. Ti/Au is evaporated and lifted off. After the channel pattern is defined, the sample is exposed to oxygen plasma to remove the graphene layer out of the channel region. For some devices we etched away the graphene channel to compare the channel current.

†On leave from Department of Electrical Engineering, University at Buffalo, State University of New York, 332 Bonner Hall, Buffalo, NY 14260, USA.

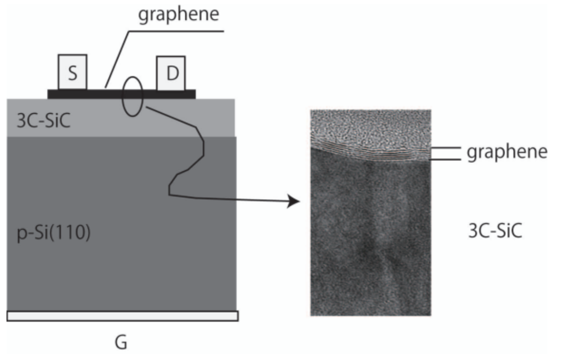

Fig. 1 Cross-sectional view of graphene transistor on Si substrate with 3C-SiC layer (left) and TEM image of epitaxial graphene on 3C-SiC (right).

3. Results and Discussion

For the fabricated epitaxial graphene sample, we confirmed few-layer graphene (FLG) was formed at the SiC surface by evaluating the sample surface with a Normarski microscope and Raman-scattering microscopy (Renishaw, Ar 514 nm) [5]. The transmission electron microscope (TEM) image of the epitaxial graphene sample's cross-section is shown in Fig. 1(right). The electrical property is characterized for a 10-μm-wide graphene channel with an 11-μm source-drain separation. A significant amount of gate leakage current is observed in this sample, indicating that the measured drain current (I_D) includes the drain-to-source current (I_{DS}) and the drain-to-gate current (I_{DG}) as shown in Fig. 2. To calculate the drain-to-source current (I_{DS}), we need to extract I_{GD} from I_D. Assuming that I_{GS} is independent of V_{DS} at a fixed gate voltage, the I_{GD} can be modeled as shown in eq. 1 below,

$$I_{DS} = I_D + I_{GD} = I_D + I_G - I_{GS} = I_D + I_G + I_{S0} \quad (1)$$

where I_{S0} is the source current when there is no biased drain voltage (V_{DS}=0). The extracted I_{DS} versus V_{DS} at the gate voltage (V_G) ranging from 0 to 0.5 V is shown in Fig. 3. The device behaves as a n-type transistor with the backgate modulation. For comparison we also measured I_{DS} in the reference device of which graphene channel was etched away by oxygen plasma. The obtained I_{DS} is negligibly small and exhibits no current modulation by the gate voltage. When the device is operated in the linear

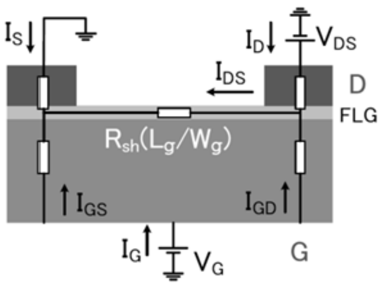

Fig. 2 A schematic of current flow distribution in the backgate FLG FET.

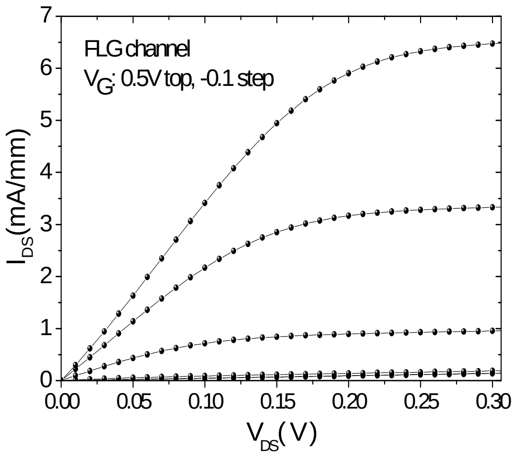

Fig. 3 Drain-to-source current (I_{DS}) versus drain-to-source voltage (V_{DS}). The result shows a n-type transistor behavior.

region, the effective mobility in the channel μ_{eff} is expressed by $\mu_{eff} = [R_{sh}C_{SiC}|V_G - V_T|]^{-1}$, where R_{sh} is the sheet resistance of the graphene channel, $C_{SiC} = \varepsilon_{SiC}/t_{SiC}$ is the insulator-layer capacitance per unit area with SiC permittivity (ε_{SiC}) of $9.72\epsilon_0$ and SiC thickness (t_{SiC}) of 80 nm, and V_T is the threshold voltage [7]. R_{sh}(shown in Fig. 4 as a function of V_G from 0.1 to 0.5 V) is obtained from the slope of the I_{DS}-V_{DS} characteristics at V_{DS} of 10-50 mV. The sheet carrier density in the FLG channel n_s is also estimated using $n_s = q^{-1}C_{SiC}|V_G - V_T|$, where q is the electron charge. The estimated sheet carrier density is in the order of 10^{11}/cm^2 as shown in the inset in Fig. 5. The estimated effective mobility has value from 432 to 6216 cm^2/(V.s) with the gate voltage from 0.1 to 0.5 V as shown in Fig. 5. The results suggest that the carrier mobility in our transistor exceeds the universal mobility of silicon in most of range.

4. Conclusion

Epitaxial-graphene-channel field-effect transistors on Si substrates are fabricated and characterized. Even though a large amount of gate-leakage current is observed, the extracted I_{DS}-V_{DS} characteristics exhibit the current modulation by the backgate bias voltage. The estimated carrier mobility exceeds the universal mobility of silicon. Although further study is needed to improve the insulating SiC layer, the results show graphene is a promising material for electronic devices in the future.

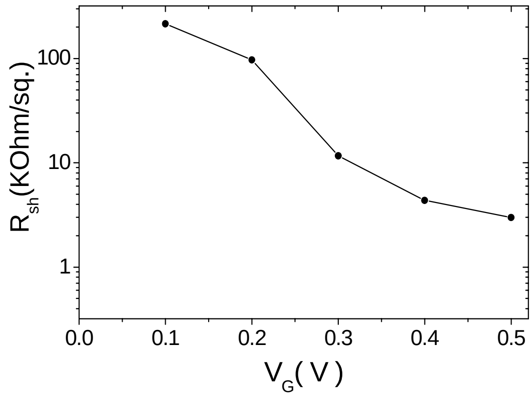

Fig. 4 Sheet resistance of the graphene FET channel as a function of V_G.

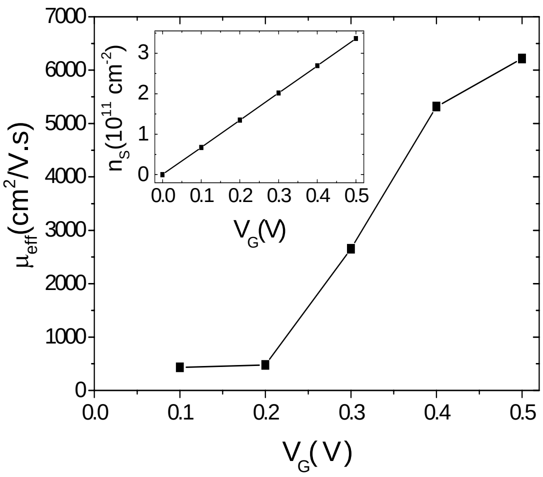

Fig. 5 Effective mobility of the graphene channel has value higher than the universal mobility of silicon in most of the range of V_G. The inset shows the sheet carrier density has values in the order of 10^{11}/cm^2 for V_G ranging from 0.1 to 0.5 V.

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