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# Effect of post thermal annealing of ZnO-TFTs by atomic layer deposition

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## 1. Introduction

Amorphous (a-Si:H) and polycrystalline silicon (poly-Si) have been widely used for the active channel layer in thin film transistors (TFTs). However, there are a number of drawbacks in these materials, such as, high temperature fabrication process and their limited performance. In recent years, the application of zinc oxide (ZnO) thin film as an active channel layer in TFT has become of great interest owing to its specific characteristics. ZnO is wide band gap (~3.37eV), transparent to visible wavelengths, and the ability to fabricate good quality films over large areas at low temperature suggests compatibility with plastic or flexible substrates [1)]. Field-effect mobility of ZnO-TFTs has recently been demonstrated as higher than that of a-Si:H TFTs. However, there is one of the serious problems is remained. That is the issue of stability.

An atomic layer deposition (ALD) method is one of the thin film preparation technologies, which attracts much attention in LSI industry. The ALD thin film is deposited with alternating exposures of a source gas and an oxidant. The ALD film has additional features of accurate thickness control, high conformity, and uniformity over large areas, because of the alternating gas supply.[2)] Further, it is reported that the TFTs with ALD thin film as the channel layer demonstrated high mobility. [3)]

In this study, we fabricated TFTs using ZnO thin film as the channel layer deposited by ALD, and evaluated their reliability.

## 2. Experiment

The ZnO thin films with thickness of 30 nm were deposited on p-type Si (100) substrates by plasma enhanced ALD using alkyl-Zn, and oxygen radical at substrate temperature of 100℃. The $SiO_2$ gate insulators, 50 nm in thickness were prepared by thermal oxidation method. Silicon substrate was used as the gate electrode. The source/drain (S/D) electrodes using Ti was patterned by lift-off technique, and fabricated bottom-gate ZnO TFTs as shown in Fig. 1. The fabricated TFTs were annealed at 100～500℃, 1hour, $O_2$ ($O_2$ =20%, $N_2$=80%) atmosphere, and their electrical properties were measured using semiconductor parameter analyser. In addition, we applied bias stress on fabricated TFTs, and measured their bias stress stability. Further, depth profiles of the films were examined by secondary ion mass spectrometry (SIMS).

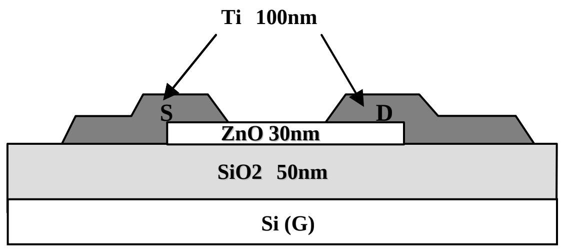


Fig.1. Bottom-gate ZnO TFT

## 3. Result and discussion

*Electrical characteristics*

We measured the electrical properties of annealed and non-annealed ZnO-TFTs. The change of transfer characteristics and drain current ($I_d$) as a function of $O_2$ annealing temperature are shown in Fig.2(a) and (b),

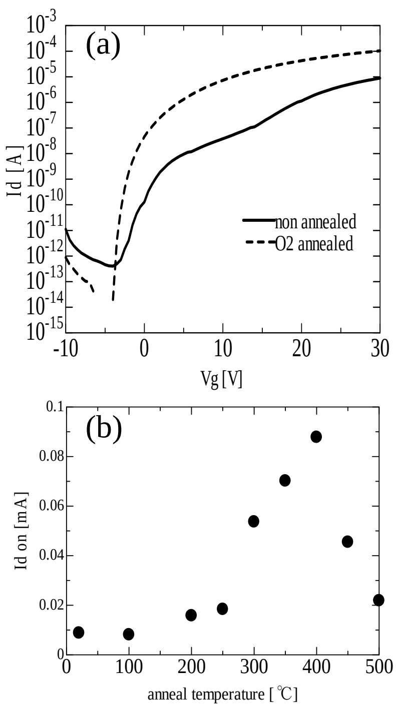


Fig.2. (a) $I_d$-$V_g$ characteristics non-annealed and annealed at 350℃, $O_2$ ambient. (b) $I_{d\,on}$ of ZnO-TFTs annealed at $O_2$ ambient as a function of annealing temperature. ($V_d$=5 V)

respectively. Both measurements were performed at $V_d$ = 5V. The off-current ($I_{d\ off}$) of ZnO-TFT annealed at 350℃ was 2.0×$10^{-14}$ A. The on/off ratio was 5.2×$10^{9}$. The field effect mobility was about 2.13 $cm^2$/Vs, the threshold voltage ($V_{th}$) was 3.2 V, and the subthreshold swing (SS) was 0.22 V/dec. We suppose that the decrease of $I_{d\ on}$ at 450℃ are due to oxidation of Ti as S/D electrodes.

The measurement of electrical properties in TFT annealed in $O_2$ ambient suggested that the oxygen deficiencies were reduced by the introduction of oxygen during the annealing.

*Bias stress stability*

We measured transfer characteristics of the fabricated TFTs after 1, 10, 100, 1000, 10000 seconds application of $V_g$/ $V_d$ = 20/20 V. Bias stress stability of the TFTs annealed at $O_2$ ambient, 300°C and 400°C were shown in Fig.3(a) and (b), respectively. The $V_{th}$ was positively shifted approximately 1.5 V after 10000 seconds stressing in the TFT annealed at 300°C. However, the $V_{th}$ shift was remarkably reduced by annealing at 400°C as shown in the Fig.3(b). We suppose that the decrease of $V_{th}$ shift was attributable to the compensated deficiencies in ZnO thin film.

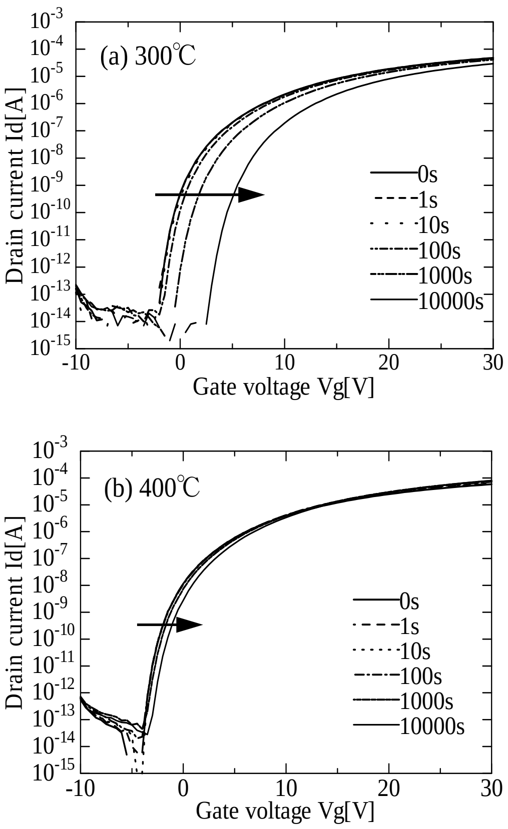


Fig.3. Bias stability (Vg/Vd=20/20) of ZnO-TFT (a) annealed at 300°C, (b)annealed at 400°C, in $O_2$ ambient (Vd=5V)

*SIMS measurement*

SIMS measurements were performed for the ZnO film annealed in $O_2$ ambient at 300℃ and 400℃ as shown in Fig.4(a) and (b), respectively. In the sample annealed at 400℃, decrease of hydrogen was observed. It is considered that the remaining hydrogen was released by the annealing. These results suggest that the hydrogen plays an important role for the improvement of reliability.

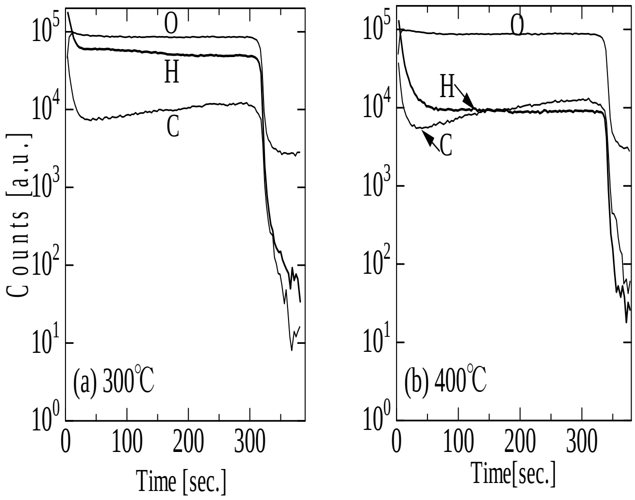


Fig.4. SIMS composition profiles of ZnO films (a) annealed at 300°C, (b) annealed at 400°C, in $O_2$ ambient

## 4. Summary

We deposited ZnO thin films as the channel layer in TFT by plasma enhanced ALD at low temperatures. Fabricated ZnO TFTs were annealed at various temperatures in ambient gas. The changes of their electrical properties were measured. TFTs with post thermal annealing in $O_2$ ambient exhibited good transistor performance. Furthermore, ZnO TFT annealed at 400℃ showed low $V_{th}$ shift against the bias stress. SIMS analysis revealed marked decrease of hydrogen by the annealing at 400℃. Through this study, we found that electrical performance were dependent on the annealing temperature and threshold voltage shift by the stress are caused by the remaining hydrogen.


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### Reference


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