Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp960-961

Low Voltage Operation of Inverted Staggered Amorphous Indium Gallium Zinc Oxide Thin Film Transistor with Al_2O_3 High-k Dielectric Material.

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1. Introduction

Indium Gallium Zinc oxide (IGZO) is one of the promising amorphous oxide semiconductor (AOS) materials well suited for fabricating switching devices in the active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diodes (AMOLED) due to the superior electronic transport properties and transparent optical characteristics in visible wavelength range compared to a-Si:H for thin film transistors (TFTs) [1]. Recently, high-k dielectric materials such as HfO_2, TiO_2, $Ba_{0.5}Sr_{0.5}TiO_2$, and Y_2O_3 grown by ALD (atomic layer deposition) have been investigated for TFTs having IGZO deposited by RF magnetron sputtering to realize devices with low threshold voltage and low leakage current [2-5]. Another prevalently used high-k dielectric material, Al_2O_3, deposited by ALD has been investigated only for the IGZO TFTs having channel deposited by utilizing DC sputtering system. In the fabrication of TFTs with inverted staggered structures, ion bombardment during the sputtering process may cause damage on the gate dielectric material, which can degrade the device performance. In this study, RF magnetron facing target sputtering (FTS) method is employed to minimize the possible electrical and physical damage on the gate dielectric material during the sputtering process. The effect of post annealing process on the performance of TFTs employing high-k Al_2O_3 as gate dielectric material is also investigated.

2. Device Fabrication

Glass coated with 150-nm-thick indium tin oxide (ITO) was used as the starting substrate. After the gate patterning, 53-nm-thick Al_2O_3 was deposited by ALD. The dielectric constant, ε_r of Al_2O_3 was measured by using MIM structures and was found to be ~8.85±0.1 as shown in Fig. 3. IGZO channel material of 50 nm was subsequently deposited by using a RF magnetron sputtering system with FTS scheme under the RF power of 350 W, a working pressure of 6 mTorr, and pure argon atmosphere. Source and drain contacts were made by e-beam evaporated Ti/Au metallizations. The schematic cross-sectional view and the SEM plane view image of the fabricated TFTs are shown in Figures 1 and 2, respectively.

3. Results and Discussions

Both the XRD patterns shown in Fig. 4. were obtained from the IGZO film annealed at 300°C for 35 min and the as-fabricated film. They exhibit the similar characteristics, which implies that the IGZO film maintains amorphous nature even after the post-annealing process. The fabricated devices were subjected to post-annealing process at variable temperatures for 35 min. From the transfer characteristics of devices shown in Fig. 5, it can be noticed that the devices begin to degrade when they are annealed at temperatures higher than 300°C. The post-annealing temperature was chosen to be 250°C and the annealing time was varied to find the optimum annealing condition. The transfer characteristics of the devices annealed at 250°C for variable time were presented in Fig. 6. and the parameters of the device characteristics were tabulated in Table 1. The device performances improved as the annealing time was inceased up to 35 min. The devices annealed at 250°C for 35min exhibits enhancement-mode characteristics and very good pinch-off characteristics as shown in Figures 7 and 8. The drain current at V_g=0 V is only in the pA range. The off – current was found to be limited by gate leakage currents, which were 28, 70, and 82 pA at the drain bias of 6 V for devices with W/L ratios of 5/5, 10/5, and 20/5, respectively. All the devices were found to be enhancement-mode and they exhibited low threshold voltage less than 2V. Threshold voltage was further reduced from 1.9 to below 0.9 V for the devices annealed at 250°C for 35 min regardless of the W/L ratios as shown in Fig. 9. The sub threshold voltage swing also improved from 0.95 to 0.25 V/decade and the saturation mobility increased from 0.1 to 4.9 cm^2/Vs by the effect of post-annealing process. Performance enhancement can be ascribed to the improved ohmic contacts of Ti/Au onto the IGZO and the reduced surface states at the semiconductor-insulator interface [6-7].

4. Conclusions

IGZO-based TFTs having Al_2O_3 gate dielectric were fabricated. By employing high-k gate oxide, low gate leakage currents and low threshold voltage were achieved. The post-annealing process at 250°C simultaneously improved the device performances such as sub threshold voltage swing, the field effect mobility, and on/off current ratio more than an order of magnitude.

Acknowledgement

This work is supported by the SEAHERO program under Grant 07SeaHeroB01-03-01 and the WCU program at GIST provided by MEST (Project No. R31-20008-000-10026-0).

References

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Table 1. Performance of a-IGZO TFTs annealed at 250°C for various time.

Annealing condition	μ_{sat} (cm^2/Vs)	S (V/decade)	V_{th} (V)	ON-OFF ratio
as-deposited	0.1	0.95	1.9	~1.9×10^4
250°C, 5min	2.48	0.4	1.6	~2×10^6
250°C,10min	4.08	0.3	1.1	~ 8×10^6
250°C,20min	4.2	0.28	1.1	~8.6×10^6
250°C,35min	4.9	0.25	0.9	~1.2×10^7

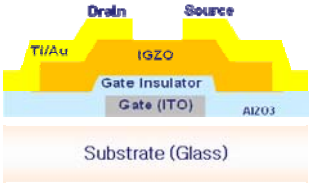


Fig. 1. Schematic cross-sectional view of the inverted staggered TFTs.

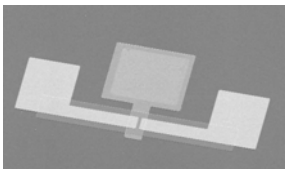


Fig. 2. SEM plane view image of the fabricated TFTs.(W/L=20/5)

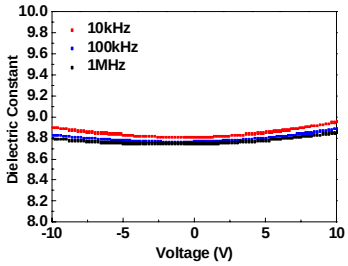


Fig. 3. Dielectric constant of Al_2O_3 measured by using MIM (Ti/Au/Al_2O_3/ITO) capacitor as a function of bias voltage and at various frequencies of 10 kHz, 100 kHz, and 1MHz.

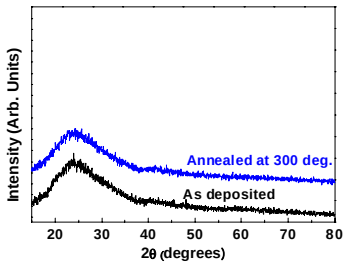


Fig. 4. XRD pattern of the as-deposited IGZO film and that of the IGZO film annealed at 300°C for 35 min.

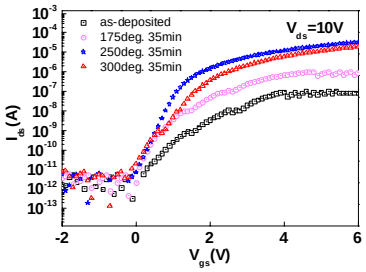


Fig. 5. Transfer characteristics of IGZO-based TFTs (W/L=20/5μm) as-deposited and annealed at various temperatures of 175, 250, and 300°C for 35 min.

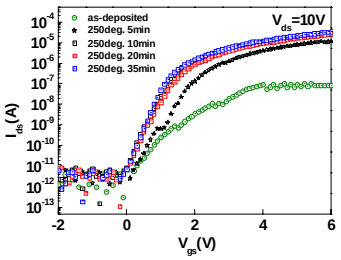


Fig. 6. Transfer characteristics of IGZO-based TFTs (W/L=20/5) after the post-annealing at 250°C for 5, 10, 20, and 35min.

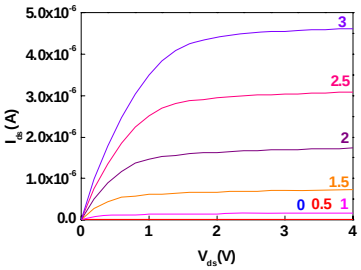
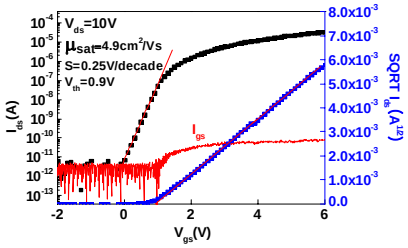
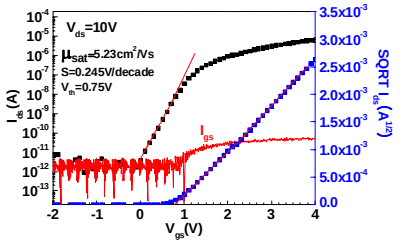


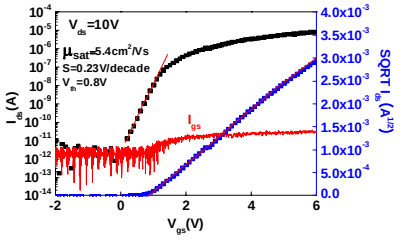
Fig. 7. Output characteristics of a typical a-IGZO TFT (W/L= 20/5) annealed at 250°C for 35 min.



(a)



(b)



(c)

Fig. 8. Transfer characteristics of the a-IGZO TFTs annealed at 250°C for 35min: (a) W/L= 20/5, (b) W/L= 10/5, (c) W/L= 5/5.

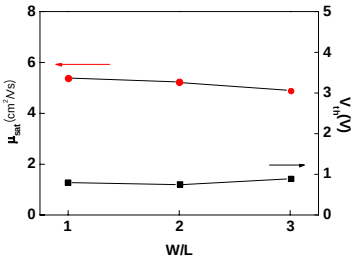


Fig. 9. Saturation field effect mobilities and threshold voltages measured after the post-annealing at 250°C for 35 min for devices with variable W/L ratios.