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Single-Electron Transport through Discrete Dopants

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1. Introduction

The interplay between single electrons and discrete impurity (dopant) atoms has attracted a wide interest for future nanoelectronics. Recent results of transport spectroscopy of isolated dopants in the channel of nanoscale field-effect transistors (FETs) shed light on the discreteness of charging effects in individual dopants [1,2]. Advances in dopant implantation techniques can further provide control over these systems [3].

From a practical viewpoint, systems of few dopants can offer a wide range of applications. We have recently demonstrated time-correlated single-electron transfer [4,5] and inter-dopant coupling modulation in nanowire FETs containing several dopants [6].

In this work, we report results on transport through discrete dopants showing the controllability of dopant-induced quantum dot (QD) array structure by channel geometry. Furthermore, using a low-temperature Kelvin probe force microscope (LT-KFM) technique [7] we observed single-electron charging events directly by monitoring the potential changes under V_{sd} application.

2. Single-electron transport characteristics in dopant-induced QDs

Ionized dopants in silicon doped nanoscale-channel FETs introduce Coulombic potential wells in the channel potential effectively working as QDs. We suggest that the length of the channel has a significant effect on the structure of the QD array, especially at the initial stages of conduction. This effect is illustrated by the potential simulations in Figs. 1(a)-1(c) obtained by superposing the Coulombic potential wells due to all dopants randomly distributed in nanowires of different dimensions. It is expected that shorter nanowires (and disk-shaped channel with radial symmetry) have a single global minimum due to the long range action of dopant potentials. At the initial stages of conduction (when source Fermi level crosses the lowest lying potential well), these devices will behave as single-QD SETs [Fig. 1(a)]. Longer nanowires have large probability of containing several global minima (several QDs) in the V_{sd} measurement window due to their axial symmetry [Figs. 1(b)-1(c)]. Statistical simulations indicate that the initial QDs typically enclose one dopant, allowing the study of single-electron transport through discrete dopants even in the presence of other dopants in the channel.

Figure 2 shows measured I_{sd}-V_{fg} characteristics for phosphorus-doped-channel SOI-FETs with the channel having different shapes and dimensions. In each figure, the full V_{fg} range and the region around the first peak are shown. Current oscillations observed in all characteristics can be ascribed to single-electron tunneling events through the dopant-induced QD arrays. The number of sub-peaks embedded in a current peak is a good indication of the number of QDs in the channel [8]. The smooth single peaks observed for disk-shaped channel FET [Fig. 2(a)] and short channel FET [Fig. 2(b)] are indication of the formation of a single QD. On the other hand, the multiple-split-peak features for longer channel FETs [Figs. 2(c) and 2(d)] prove the existence of a multiple-QD array in the channel. This trend is supported by Fig. 2(e) in which the number of sub-peaks contained in the first current peak (average value from a number of 5-10 devices) is plotted as a function of channel length.

3. Observation of single-electron charging by Kelvin probe force microscope

We measured the channel potential by using a low-temperature KFM technique. The schematic setup for the measurement is shown in Fig. 3. First, a negative voltage was applied to the back gate and side gates to deplete the channel of free carriers [7]. Then the potential inside the channel was measured with no current in the channel (V_{sd}=0 mV) and when single-electron tunneling current starts to flow ($V_{sd}\neq$0 mV). The surface potential maps measured on an area of 125×125 nm^2 (covering most part of the channel) are shown in Figs. 4(a) and 4(b), respectively. In Fig. 4(a) current does not flow and the surface potential map reflects only contributions from bare ionized dopants. Potential minima can be noticed as dark areas close to the center of the channel (marked by arrows). As we increase V_{sd}, current starts to flow and some of the electrons become trapped into dopant-induced potential wells [see Fig. 4(b)].

Figure 5 shows line profiles taken at the lowest potential position (indicated by upper arrows) as a function of V_{sd}. The depth of several tens of mV and the lateral extension of 5-15 nm of the well are in good agreement with typical characteristics of discrete phosphorus dopants in silicon (ionization energy of 44 meV and Bohr diameter of about 5 nm). We observe discrete potential changes inside the well under V_{sd} application. The potential is raised when current is allowed to flow leading eventually to a flat potential in the channel. These potential changes can be ascribed to single-electron charging of individual dopants.

Conclusions

We show results of single-electron transport through discrete dopants in nanoscale-channel FETs. We showed that the structure of dopant-induced QD array at the initial stages of conduction can be statistically controlled by channel geometry. We also directly monitored the initial single-electron charging events by KFM potential mapping of the channel under V_{sd} application.

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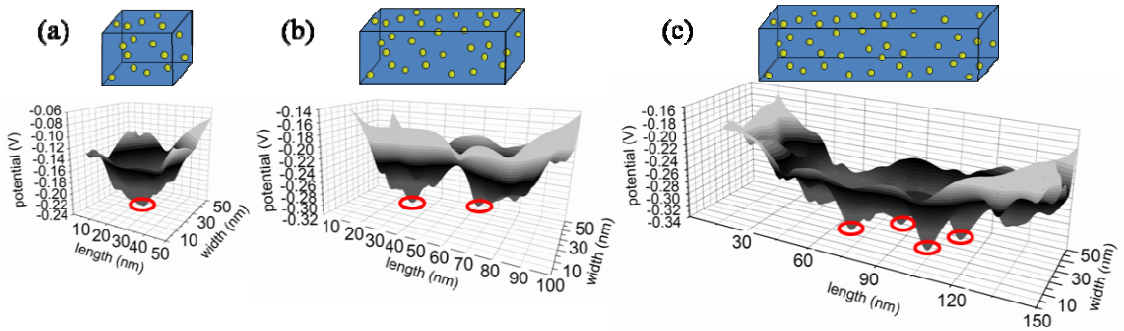

Fig. 1. Discrete dopant distribution and simulated potential landscapes for nanowire channels with same width (50 nm), but different lengths: (a) 50, (b) 100, and (c) 150 nm. Lowest potential wells are marked by circles.

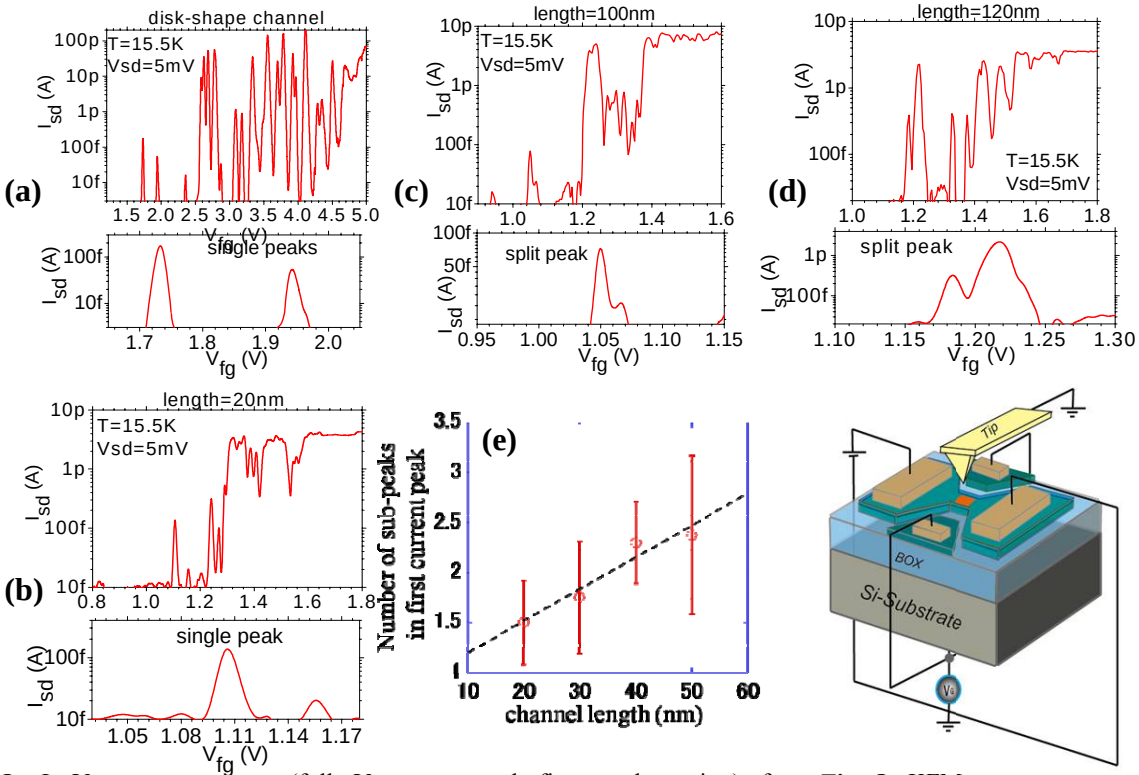

Fig. 2. I_{sd}-V_{fg} measurements (full V_{fg} range and first peak region) for doped-channel FETs: (a) disk-shaped channel; (b) nanowire (L_{ch}=20 nm); (c) nanowire (L_{ch}=100 nm); (d) nanowire (L_{ch}=120 nm). (e) Statistical results of number of sub-peaks observed in the first current peak (averaged for 5-10 devices).

Fig. 3. KFM measurement setup and biasing. Scan area covering almost completely the channel is also indicated.

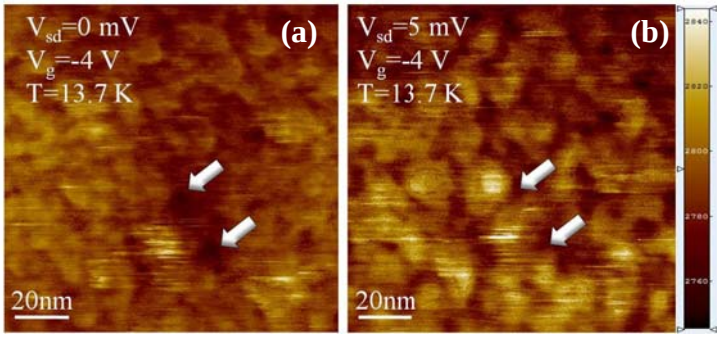

Fig. 4. Surface potential images taken by LT-KFM on the channel of doped-nanowire FET for V_{sd}= (a) 0 and (b) 5 mV. Potential wells filled by applying V_{sd} are indicated by arrows.

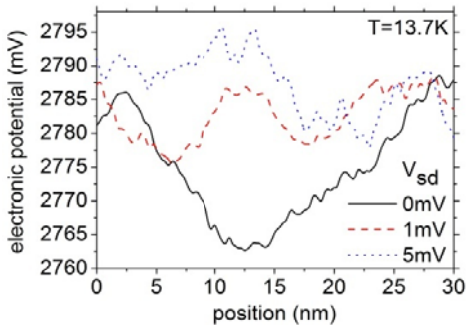

Fig. 5. Line potential profiles in the region of minimum potential (marked by upper arrow in Fig. 4) for V_{sd}=0, 1, and 5 mV.