Tunnel spectroscopy of electron subbands in thin SOI MOSFETs

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1. Introduction
It is becoming increasingly important to understand and control quantum-mechanical effects in nanoscale structures in future functional devices. This is also true for nanometer-scale silicon devices such as ultrathin-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on silicon-on-insulator (SOI) substrates, where the carriers are strongly confined in Si/SiO2 quantum wells [1]. There have been experimental studies on the quantum confinement of electrons in such a system using SOI MOSFETs [2], resonant tunneling diodes [3], and light emitting diodes [4, 5]. However, the electronic states still need to be more fully clarified to explore new applications based on the quantum effect in nanometer-scale silicon.

Here we report tunnel spectroscopy of electron subbands in thin SOI MOSFETs, where subband states consist of both in-plane four-fold and out-of-plane two-fold degenerate valleys in a SOI (001) layer. We observed clear and reproducible features in gate tunneling currents when electrons were injected into the thin SOI layer. The observed features can be well ascribed to the in-plane valley subbands having larger density of states than out-of-plane valley ones due to its effective mass anisotropy.

2. Device preparation
The devices were SOI MOSFETs fabricated on a SIMOX (001) wafer annealed at high temperature for a long time in order to minimize the influence of interfacial roughness at the Si/BOX interface [6], as shown in Fig. 1 (a). A double-layer gate structure was employed. The lower n-type poly-Si gate was used as a tunneling gate through which electrons are injected into the SOI channel with various sets of width (W) and length (L). The thicknesses of the tunneling gate oxide (tox) and the buried oxide (tbox) were about 2 and 400 nm, respectively. SOI with nominal thicknesses (tSOI) of 10 and 25 nm was prepared. The wide upper gate was used as ion implantation mask to form an n-type source and drain. We used the substrate as a back gate.

3. Experimental Results and Discussion
The lower gate’s tunneling current dILG/dVLG was measured as a function of its voltage VLG at positive back-gate voltage VBG, as shown in Fig. 2. Large positive VBG was applied to avoid electron depletion in the tunneling gate, through which electrons are injected into the channel under the lower-gate region, especially for negative VLG, so that the Fermi level of the poly-Si gate is also plotted as a thick solid line. When we compare the calculation with the experimental results, it is found that the experimental dILG/dVLG, at which the peaks were observed, are reasonably reproduced, as indicated by arrows in Fig. 2, where the gate Fermi level is aligned with the subband edge of the four-fold valleys.

In order to understand the observed structures quantitatively, we calculated the energies of electron subbands in a SOI well under given electric fields by solving Schrodinger equation based on the effective mass approximation. In this calculation, the ground subband of the two-folded valleys with the effective mass of 0.98 perpendicular to the well was assumed to be left at the Fermi level of the SOI channel for simplicity. Figure 6 shows the calculated energies with respect to the Fermi level of the channel as a function of VLG for tSOI = 8.5 nm and tSOI = 20 nm. The solid lines and the dotted lines represent the subbands arising from the four-fold valleys and the two-fold valleys, respectively. The Fermi level of the poly-Si gate is also plotted as a thick solid line. When we compare the calculation with the experimental results, it is found that the experimental VLG, at which the peaks were observed, are reasonably reproduced, as indicated by arrows in Fig. 6, where the gate Fermi level is aligned with the subband edge of the four-fold valleys.

In the present tunnel spectroscopy, tunneling current is expected to be proportional to the DOS of SOI because we use the poly-Si as an electron source with Fermi energy much smaller than metal. Since, considering the effective mass anisotropy (m_perp = 0.98, m_par = 0.19) and the valley degeneracy, the DOS of the four-fold valleys is approximately 4.5 times larger than that of the two-fold ones, the tunnel current through four-fold valleys is also expected to be 4.5 time larger and dominant.

In Fig. 7, we compare the experimental dILG/dVLG and calculated tunneling current dILG/dVLG at 0 K considering the DOS and the bias-dependent transmission probability. It is seen that the structures due to the four-fold valleys are more distinct in the calculation, and the calculation shows a good agreement in their VLG positions with the experimental results. It should also be noted that higher subbands show a larger inhomogeneous broadening in the experiment, which is consistent with our calculation, because the energy of higher subbands are more sensitive to the structural fluctuations. All these results suggest that the peak behavior observed in dILG/dVLG can be attributed to electron tunneling from the poly-Si gate to the in-plane four-fold degenerate valleys. Further detailed analysis using the self-consistent model remains as future work, especially to explain the disagreement observed in the low-bias regime. We add that the injected electrons are relaxed in the channel by the inter-subband transitions, which can be dipole allowed and therefore might be useful for light emission in silicon [4].

4. Conclusions
We observed subband-induced features in gate tunneling currents when electrons are injected into a thin SOI well. From the theoretical consideration of the quantized energy levels and their density of states, the observed features can be well ascribed to the in-plane four-fold valley subbands.

References
Fig. 1. (a) Schematic cross section of the device structure (top) and top view of the device (bottom). (b) The potential profile along top to bottom of the device. (c) Six equivalent valleys in the conduction band. With two-dimensional confinement, a Si quantum well forms a subband consisting of two-fold valleys with effective mass $m_l = 0.98$ (marked “A”) perpendicular to well and four-fold ones with $m_t = 0.19$ (marked “B”). The thicker lines in SOI region (in (b)) indicate subbands arising from four-fold degenerate valleys. Dotted lines are from the rest of the two-fold ones.

Fig. 2. $I_{LG}$ and $dI_{LG}/dV_{LG}$ curve with nominal SOI thickness of 25 nm at 20 K.

Fig. 3. $I_{LG}$ and $dI_{LG}/dV_{LG}$ curve with nominal SOI thickness of 10 nm at 20 K.

Fig. 4. Tunnel conductance $dI_{LG}/dV_{LG}$ for $(L \times W = 3 \times 4 \mu m)$ and $(0.8 \times 0.8 \mu m)$ for devices with SOI thickness of 10 nm.

Fig. 5. Temperature dependency of $dI_{LG}/dV_{LG}$ for devices with SOI thickness of 10 nm at $V_{BG} = 135$ V and $V_D = 50$ mV.

Fig. 6. Calculated energies of subbands as a function of $V_{LG}$ for $t_{SOI} = 8.5$ nm and $t_{ox} = 2.0$ nm. The solid lines and the dotted lines represent the subbands arising from the four-fold and the two-fold valleys, respectively. Arrows indicate coincidence points with the gate Fermi surface and the subbands edge originating from four-fold valleys.

Fig. 7. $I_{LG}$ and $dI_{LG}/dV_{LG}$ curve at 20 K for the device with nominal SOI thickness of 10 nm. Calculated $I_{LG}$ with $t_{SOI} = 8.5$ and $t_{ox} = 2.0$ nm are also plotted. Indexes “1” to “5” represent subband edge of four-fold valleys.