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Tunnel spectroscopy of electron subbands in thin SOI MOSFETs

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1. Introduction

It is becoming increasingly important to understand and control quantum-mechanical effects in nanostructures for future functional devices. This is also true for nanometer-scale silicon devices such as ultrathin-channel metal-oxide semiconductor field-effect transistors (MOSFETs) on silicon-on-insulator (SOI) substrates, where the carriers are strongly confined in Si/SiO_2 quantum wells [1]. There have been experimental studies on the quantum confinement of electrons in such a system using SOI MOSFETs [2], resonant tunneling diodes [3], and light emitting diodes [4, 5]. However, the electronic states sill need to be more fully clarified to explore new application based on the quantum effect in nanometer-scale silicon.

Here we report tunnel spectroscopy of electron subbands in thin SOI MOSFETs, where subband states consist of both in-plane four-fold and out-of-plane two-fold degenerate valleys in a SOI (001) layer. We observed clear and reproducible features in gate tunneling currents when electrons were injected into the thin SOI layer. The observed features can be well ascribed to the in-plane valley subbands' having larger density of states than out-of-plane valley ones due to its effective mass anisotropy.

2. Device preparation

The devices were SOI MOSFETs fabricated on a SIMOX (001) wafer annealed at high temperature for a long time in order to minimize the influence of interfacial roughness at the Si/BOX interface [6], is shown in Fig. 1 (a). A double-layer gate structure was employed. The lower n-type poly-Si gate was used as a tunneling gate, through which electrons are injected into the SOI channel with various sets of width (W) and length (L). The thicknesses of the tunneling gate oxide (t_{ox}) and the buried oxide (t_{box}) were about 2 and 400 nm, respectively. SOI with nominal thicknesses (t_{SOI}) of 10 and 25 nm was prepared. The wide upper gate was used as ion implantation mask to form an n-type source and drain. We used the substrate as a back gate.

3. Experimental Results and Discussion

The lower gate's tunneling current I_{LG} was measured as a function of its voltage V_{LG} at positive back-gate voltage V_{BG} (at a small constant drain voltage V_D and upper gate's voltage V_{UG}). Large positive V_{BG} was applied to avoid electron depletion in the channel under the lower-gate region, especially for negative V_{LG}, so that the Fermi level of the channel would be pinned to those of the source/drain (Fig.1 (b)), thereby allowing the tunnel spectroscopy of the channel. Figure 2 shows typical I_{LG}-V_{LG} and its derivative (dI_{LG}/dV_{LG}) taken at 20 K for a sample with t_{SOI} = 25 nm. The increase of dI_{LG}/dV_{LG} at $V_{LG} > 0$ reflects the monotonic increase of the transmission probability of SiO_2 tunnel barrier. Tunnel current is proportional to transmission probability and DOS of both the gate and SOI. With increasing V_{LG}, both the transmission probability and the number of electrons in SOI increase. Electrons in SOI occupy only a few lower subbands, and there are therefore almost no pronounced peaks in dI_{LG}/dV_{LG}. In contrast, small peak features can be seen in $V_{LG} < 0$ (arrowed in Fig. 2). These characteristics are also seen for the device with t_{SOI} =10 nm as shown in Fig. 3. Strikingly, the peaks at $V_{LG} < 0$ are much clearer with a larger separation. The observation of these peaks only at the negative bias, which causes the electron injection into the channel, and their t_{SOI} dependence strongly indicate that they originate from DOS structures of the thin SOI channel. The area-size dependence of dI_{LG}/dV_{LG} characteristics is shown in Fig. 4 for devices with t_{SOI} =10 nm. The samples show peaks at almost the same V_{LG}, which also suggests that the peak positions are dominated by t_{SOI}, or the vertical confinement in the channel. In contrast, the peaks become more unclear with increasing device area. This indicates that the peaks suffer from inhomogeneous broadening since it is more likely that a larger area is accompanied by a larger fluctuation in t_{SOI} or tunnel oxide thickness. This is also supported by the temperature dependence of dI_{LG}/dV_{LG} as shown in Fig. 5. While the peaks are ambiguous at higher temperature due to the thermal broadening of the Fermi surface of the poly Si gate, their sharpness is mostly unchanged below 50 K. We can therefore conclude that the inhomogeneous broadening is dominant below 50 K.

In order to understand the observed structures quantitatively, we calculated the energies of electron subbands in a SOI well under given electric fields by solving Schrodinger equation based on the effective mass approximation. In this calculation, the ground subband of the two-folded valleys with the effective mass of 0.98 perpendicular to the well was assumed to be kept at the Fermi level of the SOI channel for simplicity. Figure 6 shows the calculated energies with respect to the Fermi level of the channel as a function of V_{LG} for t_{SOI} = 8.5 nm and t_{ox} = 2.0 nm. The solid lines and the dotted lines represent the subbands arising from the four-fold valleys and the two-fold valleys, respectively. The Fermi level of the poly-Si gate is also plotted as a thick solid line. When we compare the calculation with the experimental results, it is found that the experimental V_{LG} at which the peaks were observed, are reasonably reproduced, as indicated by arrows in Fig. 6, where the gate Fermi level is aligned with the subband edge of the four-fold valleys.

The reason only the four-fold valley subbands were detected, while the two-fold ones were not, can be understood in terms of their DOS of SOI; In the present tunnel spectroscopy, tunneling current is expected to be proportional to the DOS of SOI because we use the n+ poly Si as an electron source with Fermi energy much smaller than metal. Since, considering the effective-mass anisotropy (m_l = 0.98, m_t = 0.19) and the valley degeneracy, the DOS of the four-fold valleys is approximately 4.5 times larger than that of the two-fold ones, the tunnel current through four-fold valleys is also expected to be 4.5 time larger and dominant.

In Fig. 7, we compare experimental I_{LG}, dI_{LG}/dV_{LG} and calculated tunneling current (0 K) considering the DOS and the bias-dependent transmission probability. It is seen that the structures due to the four-fold valleys are more distinct in the calculation, and the calculation shows a good agreement in their V_{LG} positions with the experimental results. It should also be noted that higher subbands show a larger inhomogeneous broadening in the experiment, which is consistent with our calculation, because the energy of higher subbands are more sensitive to the structural fluctuations. All these results suggest that the peak behavior observed in dI_{LG}/dV_{LG} can be attributed to electron tunneling from the poly-Si gate to in-plane four-fold degenerate valleys. Further detailed analysis using the self-consistent model remains as future work, especially to explain the disagreement observed in the low-bias regime. We add that the injected electrons are relaxed in the channel by the inter-subband transitions, which can be dipole allowed and therefore might be useful for light emission in silicon [4].

4. Conclusions

We observed subband-induced features in gate tunneling currents when electrons are injected into a thin SOI well. From the theoretical consideration of the quantized energy levels and their density of states, the observed features can be well ascribed to the in-plane four-fold valley subbands.

References

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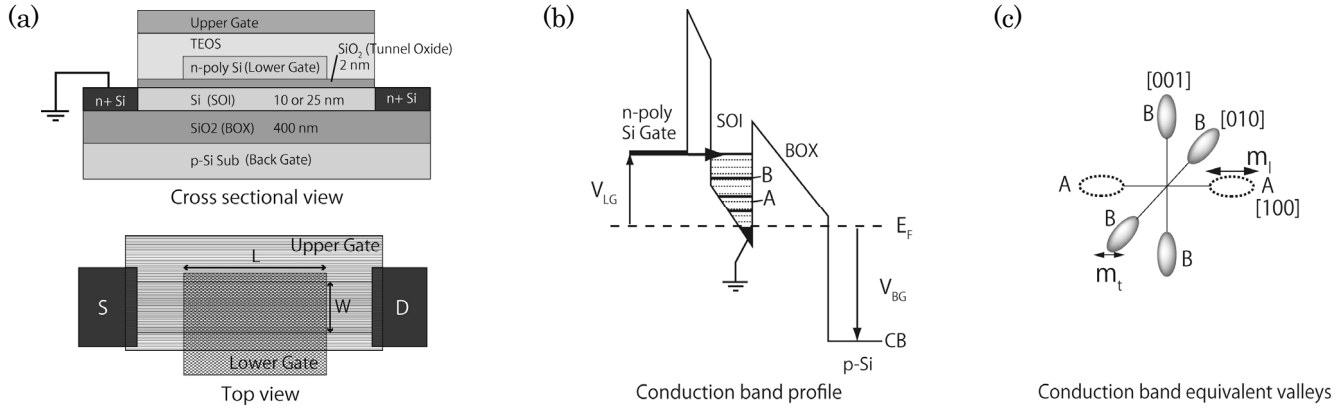

Fig. 1. (a) Schematic cross section of the device structure (top) and top view of the device (bottom). (b) The potential profile along top to bottom of the device. (c) Six equivalent valleys in the conduction band. With two-dimensional confinement, a Si quantum well forms a subband consisting of two-fold valleys with effective mass m_l= 0.98 (marked "A") perpendicular to well and four-fold ones with m_t= 0.19 (marked "B"). The thicker lines in SOI region (in (b)) indicate subbands arising from four-fold degenerate valleys. Dotted lines are from the rest of the two-fold ones.

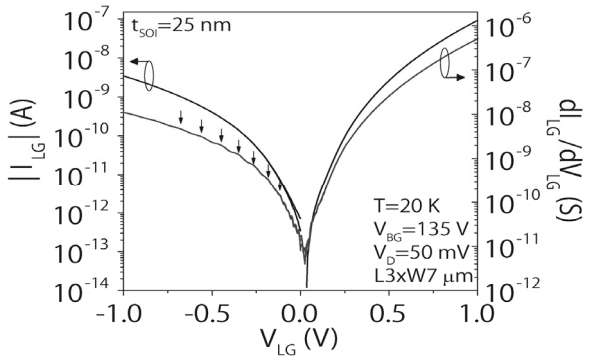

Fig. 2. I_{LG} and dI_{LG}/dV_{LG} curve with nominal SOI thickness of 25 nm at 20 K.

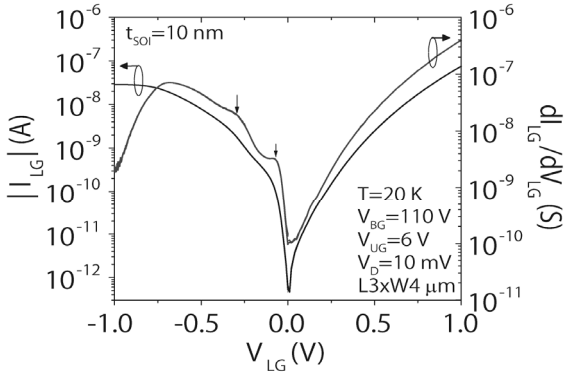

Fig. 3. I_{LG} and dI_{LG}/dV_{LG} curve with nominal SOI thickness of 10 nm at 20 K.

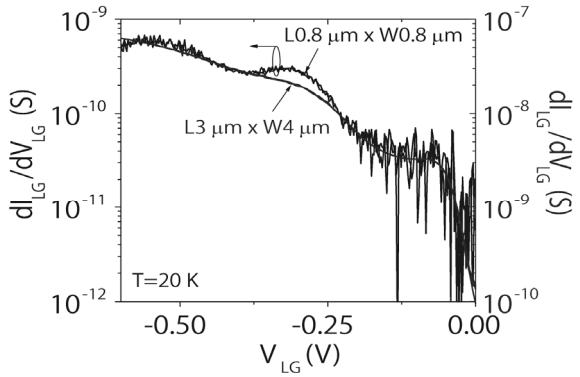

Fig. 4. Tunnel conductance dI_{LG}/dV_{LG} for (L x W = 3 x 4 μm) and (0.8 x 0.8 μm) for devices with SOI thickness of 10 nm.

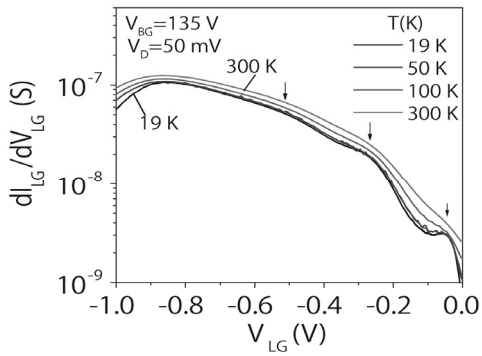

Fig. 5. Temperature dependency of dI_{LG}/dV_{LG} for devices with SOI thickness of 10 nm at V_{BG}= 135 V and V_D = 50mV.

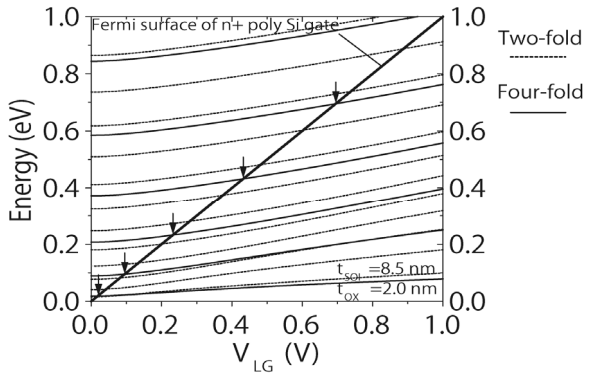

Fig. 6. Calculated energies of subbands as a function of V_{LG} for t_{SOI}= 8.5 nm and t_{ox}= 2.0 nm. The solid lines and the dotted lines represent the subbands arising from the four-fold and the two-fold valleys, respectively. Arrows indicate coincidence points with the gate Fermi surface and the subbands edge originating from four-fold valleys.

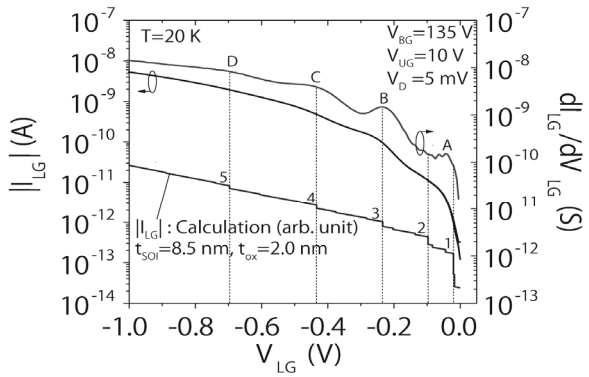

Fig. 7. I_{LG} and dI_{LG}/dV_{LG} curve at 20 K for the device with nominal SOI thickness of 10 nm. Calculated I_{LG} with t_{SOI} = 8.5 and t_{ox} = 2.0 nm are also plotted. Indexes "1" to "5" represent subband-edge of four-fold valleys.