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Dislocation-Based Si-Nanodevices

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1. Introduction

There are numerous discussions on future strategies of CMOS device scaling [1, 2]. According to simulations, the ultimate MOSFET is characterized by gate lengths below 10 nm [2, 3]. Devices with gate lengths up to about 15 nm were already demonstrated using existing technologies [4, 5], which, however, are not feasible for smaller dimensions. Recently, silicon nanowires were used to demonstrate transistors with dimensions of a few nanometers [6]. But there is no assembly method available to implement nanowires to real devices. On the other hand, dislocations are extended, 1-dimensional imperfections in crystalline solids or, in other words, native nanowires, showing numerous outstanding electrical properties [7, 8]. Using specific preparation methods planar arrays of such dislocations can be reproducibly prepared allowing the realization of devices with dimensions of a few nanometers in a CMOS-compatible process. First measurements on SOI MOSFETs having a planar dislocation network in the channel region proved an increasing conductance resulting in drain currents about a factor of 100 higher than in comparable layers without dislocations [7]. While previous experiments used networks with a high density of dislocations, the present paper describes a technique and first measurements on devices including only a few dislocations in the channel region.

2. Results

Properties of dislocations

Dislocations are 1- dimensional defects, i.e. their diameter is in the order of 1 nanometer. Fig. 1 presents a high-resolution cross-section electron microscope image of typical dislocations formed at a Si-Si bonded interface. The length of the dislocation in a misfit network is defined by the mesh size and can be up to several micrometers.

Dislocations contain a number of irregularities along the dislocation line, such as kinks and jogs, and by the ubiquitous presence of impurities close to or in the dislocation core. All these defects cause states in the forbidden gap of Si which can be occupied in n-type silicon with electrons forming a negative line charge. To keep space charge neutrality the negatively charged dislocation line is surrounded by ionized (positively charged) donor atoms, the so-called Read cylinder [8]. In the opposite case of p-type Si the dislocations form positively charged lines surrounded with ionized (negatively charged) acceptor atoms. A consequence of the dipole formed is the bending of the conduction and valence bands, i.e., the appearance of a barrier in the energy band diagram, associated with the occurrence of an electric field reaching values around 10^4 Vcm^{-1}.

Conductance of dislocations

Two-dimensional arrays of dislocations (dislocation network) are produced by wafer bonding of {100}-oriented substrates using hydrophobic surfaces [9]. A dislocation network is formed in the bonding interface, where the dislocation distance is controlled by the twist and tilt angle, respectively. Twist angles of $\vartheta_{twist} \leq$ 0,0008° result in dislocation distances of more than 1µm allowing in principle the preparation of devices with only 1 dislocation in the channel region. This can reproducible be achieved by alignment techniques for the wafer bonding process. Such dislocation networks were produced by wafer bonding of SOI wafers (150 mm in diameter) having initial thicknesses of the device layers of 15 nm (p-type, ρ = 13 – 20 Ωcm). The handle wafer and BOX layer of one of these wafers were removed resulting in a final SOI wafer with a dislocation network within a 30 nm thick device layer (Fig. 2). Using lithographic techniques and dry etching the channel region was defined. Because dislocations are parallel to <110>- directions in Si, they are parallel to the channel.

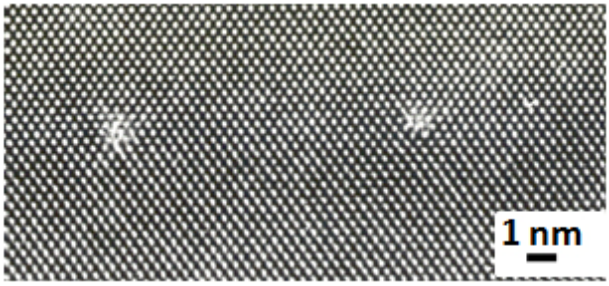

Fig. 1 High-resolution electron microscope image (cross-section image) of dislocations in a bonded interface.

Contact areas and device channels were defined by lithography techniques and reactive ion etching (RIE). Two different types of contacts were fabricated: 1) Schottky contacts were formed either by Al deposition or by nickel mo-

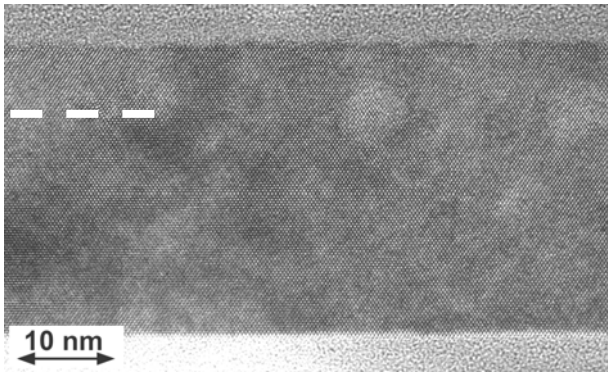

Fig. 2 TEM cross-sectional image of a 30 nm thick device layer (SOI wafer) containing a dislocation network. The network is about 10nm below the surface. The dotted line marks the bonded interface.

nosilicide (NiSi); 2) Ohmic contacts were formed by As^+ implantation (5 keV, $1{\cdot}10^{15}cm^{-2}$) combined with a RTA step (950°C, 60 sec.).

Conductance measurements

Fig. 3 shows the conductance of the dislocation layer by measuring I-V curves between two n^+-Ohmic contacts. An increase of the current I by 6 orders of magnitude is obtained for the layer having dislocations compared to a reference sample prepared on a SOI wafer with the same device layer thickness. The increase of I depends on the dislocation density and probably on the type of the dislocations. The reason is that dislocations form channels of higher conductance in the silicon layer resulting in a higher carrier concentration in the channel [7] but increase also the effective carrier mobility which is consistent with quasi-ballistic transport along dislocations [10]. From Fig. 3, we can see that the transport carriers in the dislocations are

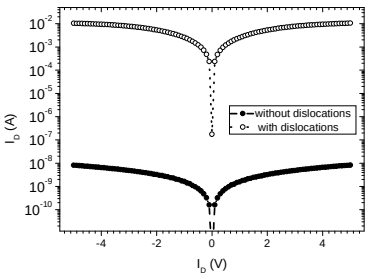

Fig. 3 I-V characteristics of 2 n^+- contacts on SOI with and without dislocations. The length between contacts is 5 µm, while the width is 1µm. Because the dislocation distance is about 150 nm, about 6 dislocations are present in the channel.

electrons. With 2 n^+-Ohmic contacts, an n^+-n-n^+ transport path through dislocations is formed, which results in a higher conductance. However, on the SOI substrate without dislocation, an n^+-p-n^+ structure allows only a much lower current.

Fig.4 shows the I-V characteristics between two Al contacts. On the SOI wafer without dislocations, two back-

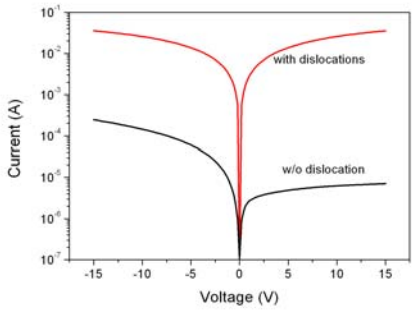

Fig.4 I-V characteristics between two Al Schottky contacts on SOI with and without dislocations.

to-back Schottky diodes are formed. The currents shown in Fig. 4 represent the reverse currents of a Schottky contact. For the layer with dislocations, the currents are much higher. The currents consist of 2 contributions. One is from the reverse Schottky contact to the p-Si layer, the other from the electron current along the dislocations. The latter dominants the currents because the reverse currents of the Schottky contact are small, as indicated by the I-V curves from the SOI layer without dislocations. This further proves that the dislocation is highly conductive. A high density of negative charges is located on dislocations.

3. Conclusions

SOI layers with dislocation networks have been fabricated using wafer bonding. The conductance of dislocations was characterized by measuring the currents through two Ohmic contacts or two Schottky contacts. Negative charges in the dislocation have been proved from the measurements. Dislocations show very high conductance with 6 orders of magnitude higher than that of a comparable SOI layer.

References

[1] D.A. Antoniadis and A. Khakifirooz, *IEDM Techn. Digest* (2008) 253.

[2] W. Haensch, E.J. Nowak, R.H. Dennard, P.M. Solomon, A. Bryant, O.H. Dokumaci, A. Kumar, X. Wang, J.B. Johnson, and M.V. Fischetti, IBM J. Res. & Dev. **50** (2006) 339.

[3] R. Venugopal, S. Goasguen, S. Datta, and M.S. Lundstrom, J. Appl. Phys. **95** (2004) 292.

[4] R. Chau, B. Boyanov, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, Physica **E19** (2003) 1.

[5] T. Ernst, L. Duraffourg, C. Dupré, E. Bernard, P. Andreuucci, S. Bécu, E. Ollier, A. Hubert, C. Halté, J. Buckley, O. Thomas, G. Delapierre, S. Deleonibus, B. de Salvo, P. Robert, and O. Faynot, *IEDM Techn. Digest* (2008) 745.

[6] G. Zheng, W. Lu, S. Jin, and C.M. Lieber, Adv. Mater. **16** (2004) 1890.

[7] A. Ishikawa, C. Yamamoto, and M. Tabe, Appl. Phys. Lett. **88** (2006) 073112.

[8] M. Kittler and M. Reiche, Adv. Engin. Mat. **11** (2009) 249.

[9] M. Reiche, Mater. Sci. Forum **590** (2008) 57.

[10] M. Lundstrom and J. Guo, *Nanoscale Transistors*, Springer, New York (2006).