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TFT-type Flash Memory with Biomineralized Nanodots on SOI Substrate

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1. Introduction

System-on-panels (SOP) have attracted much attention as next generation display, and many researches on the thin film transistor (TFT) have been carried out. However, very few papers on the TFT-type memories have been reported. Fabrication of high-performance thin film memories is important to realize a SOP.

Meanwhile, floating gate memories have attracted much attention as high-performance and low energy consumption nonvolatile memory. We have fabricated a floating nanodot gate memory by using cage-shaped supramolecular protein, ferritin, as shown Fig. 1. [1] The fabricated bionanodot (BND) floating gate memory showed clear memory operation due to the charge confinement in the embedded BND. Moreover, a TFT-type flash memory was fabricated by using ferritin on poly-Si crystallized by solid phase crystallization (SPC). [2] However, the process temperature of this flash memory was up to 600 ^{o}C, relatively high temperature. To fabricate high-performance TFT-type flash memory at low temperature, we proposed the fabrication of the TFT-type flash memory on a SOI substrate by using supramolecular protein.

2. Experimental details

Si islands were patterned on SOI by reactive ion etching (RIE). Source and drain regions were formed by P ion implantation. A 3-nm-thick layer of SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) as a tunnel oxide. A monolayer of 3-aminopropyltriethoxysilane (APTES) was formed on tunnel oxide by vapor deposition to enhance an adsorption of ferritin. A 1.0 mg/ml of Co-bionanodot (Co-BND) accommodated ferritin solution, which containing 25 mM 2-(N-morpholino) ethane sulfonic acid (MES) and tris (hydroxylmethyl) aminomethane (Tris) was cast on the APTES, and then the excess solution was removed with pure water to prevent the formation of a ferritin multilayer. The outer shell of ferrtin was removed by ultraviolet irradiation in an ozone atmosphere at 115 ^{o}C for 60 min. A 20-nm-thick layer of SiO_2 was deposited by PECVD as control gate oxide, and Ti electrode was deposited on the SiO_2 layer. The fabricated memory was annealed at 450 ^{o}C for 1 h in a reductive gas mixture (10% H_2 and 90% N_2) to improve metal contact and reduce Co-BND. Figure 2 shows a cross-sectional diagram of the fabricated memory. Cores were embedded completely in the gate oxide. The gate width and gate length were 5 μm and 3 μm, respectively.

3. Result and discussion

Figure 3 shows a scanning electron microscope (SEM) image of Co-BNDs on the tunnel oxide surface after removing the outer shell of ferritin. The adsorption density of the Co-BND array was estimated from the SEM image to be as 7.4×10^{11} on SiO_2, corresponding to over 80 % of the theoretical density of 8.0×10^{11} cm^{-2}.

Figure 4 shows the I_D-V_G characteristic of the fabricated TFT without Co-BND. An I_D-V_G curve without hysteresis was observed. The threshold voltage, mobility and S factor were -0.92 V, 271 cm^2/ (V•s) and 0.16 V/decade, respectively. Figure 5 shows the I_D-V_G characteristic of the fabricated TFT-type flash memory. An I_D-V_G curve with hysteresis was observed. This hysteresis was caused by the injection of electrons into Co-BNDs and their ejection. The width of the hysteresis was 3 V.

The charge retention characteristic was measured by monitoring the change in the memory window at -1 V after writing at +8 V and erasing at -13 V with 1s pulsed bias. We measured the difference between the drain currents after writing and erasing over 10^4 s. Figure 6 shows charge retention characteristic of the memory. We measured the difference between the drain currents after writing and erasing over 10^4 s.

The charge storage capacity and retention characteristic of the memory with Co-BNDs can be explained on the basis of the charge confinement in the potential well of a Co-BND and the band structure of SiO_2. Figure 7 shows the band diagram of the memory during electron injection and ejection. Since the band offset of SiO_2 is 3.1 eV [3] and tunnel oxide is 3 nm, the electrons are injected into and ejected from the Co-BNDs by direct tunneling. The work function of metal Co, 5.0 eV, is positioned at the valence band of Si energy bands [1]; thus, we can expect charge retention in metal Co.

4. Summary

We fabricated TFT-type flash memory on SOI substrate at low temperature by using supramolecular protein. The fabricated memory showed clear memory and charge retention characteristic. This memory showed the possibility of the fabrication of the high-performance memory on glass and plastic substrates at low temperature.

References

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[2] K. Ichikawa et al, J. Korean. Phys. Soc, Vol. 54, No. 1 (2009) pp. 554
[3] J.Robertson et al, J. Appl. Phys. 100 (2006) 014111
[4] K. Ichikawa et al, J. Korean. Phys. Soc, Vol. 49, No. 2 (2006) pp. 569

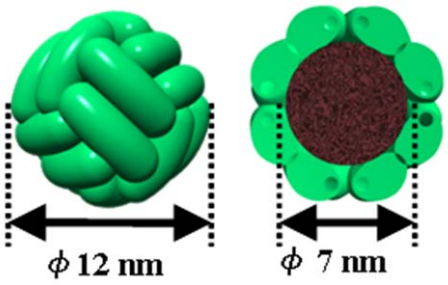

Figure 1. Ferritin

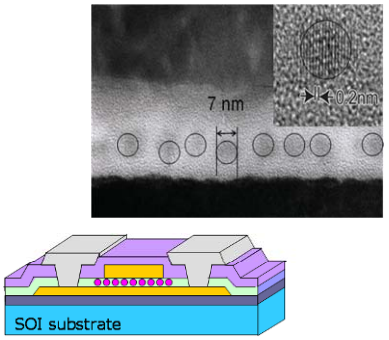

Figure 2. Cross-sectional diagram of the fabricated memory

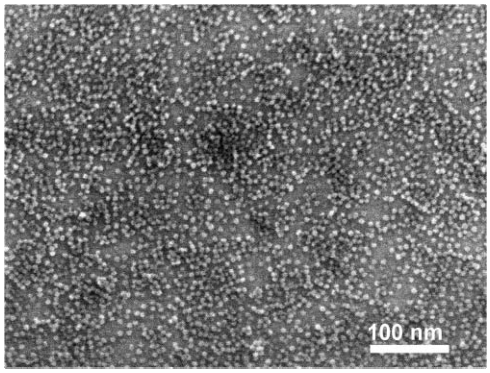

Figure 3. SEM image of Co-BND on the SiO_2 layer

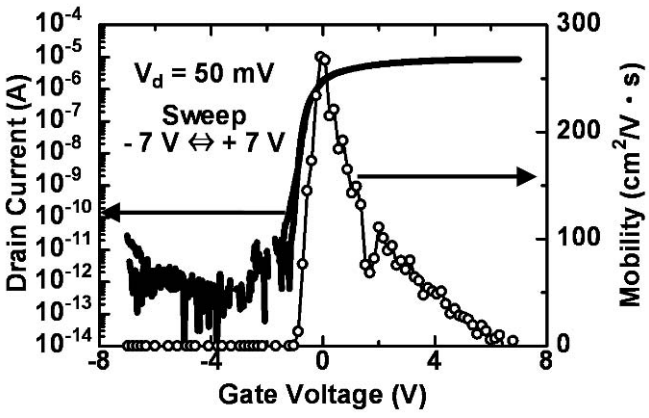

Figure 4. I_D-V_G characteristic of the TFT

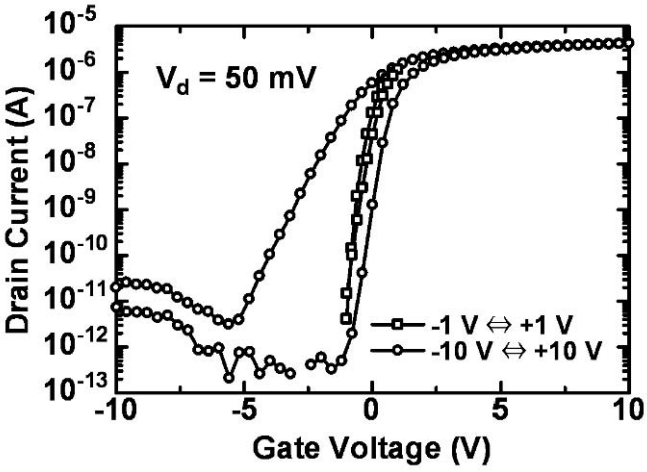

Figure 5. I_D-V_G characteristic of the fabricated memory

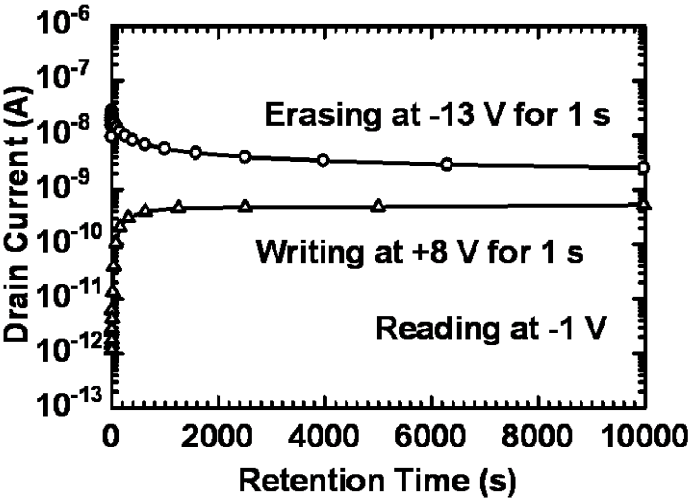

Figure 6. Retention characteristic of the fabricated memory

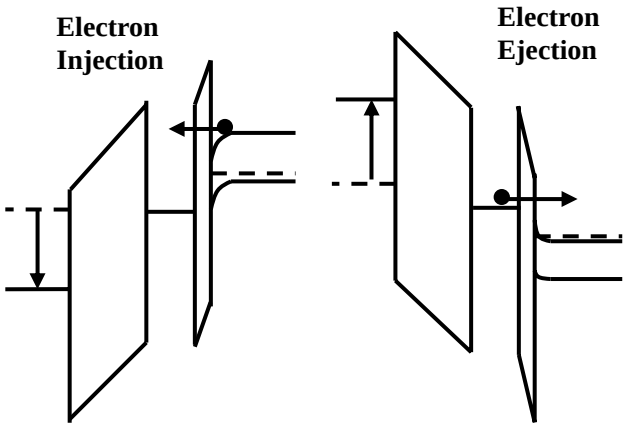

Figure 7. Band diagram of the fabricated memory