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Device Design Schemes and Electrical Characterization of Nonvolatile Memory Thin-Film Transistors with the Gate Structure of Al/P(VDF-TrFE)/Al_2O_3/ZnO

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1. Introduction

Ferroelectric polymer-based nonvolatile (NV) memory device has very attractive features such as low-cost and low-temperature process for the new fields of transparent & flexible electronics. One of the most typical polymeric ferroelectrics is poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] copolymer. Although some encouraging results have been reported on the memory devices of capacitors and/or transistors using P(VDF-TrFE) [1-2], there remains critical technological issues such as stable programming with lower voltage and longer retention time owing to its larger coercive field of the thin film.

We propose the NV memory thin-film transistor (MemTFT) employing ZnO and P(VDF-TrFE) as a semiconducting channel and a ferroelectric gate insulator, respectively, in which a thin Al_2O_3 layer is introduced between them to protect the ZnO channel during the process and to reduce the leakage current of the gate stack. This MemTFT provides a transparency in visible range and process compatibility to the flexible substrate below 200°C. However, the gate-stack should be carefully designed for the low-voltage programming. In this work, we investigate the operating point of MemTFT by a load-line analysis and characterize the fabricated device. The MemTFTs showed excellent memory and transistor performances.

2. Device Structure & Operating Point Analysis

Fig. 1(a) describes the device structure of the proposed MemTFT. The operating points can be estimated by Q (induced charge density) - V (applied voltage across the gate stack) relationship in the serially-connected capacitors. We have to note that the thickness of ZnO for the TFT actions is so thin that the channel can be fully depleted and remains as an insulating layer at negative voltage range (OFF state). The total required programming voltages for the ON (V_{on}) and OFF (V_{OFF}) operations are determined as summation of the applied voltages to P(VDF-TrFE) (V_F), Al_2O_3 (V_{ox}), and the depletion layer of ZnO channel. Therefore, a load-line on V_F axis, which is defined by $Q_o=C_o(V-V_F)$ (where Q_o corresponds to the charge density induced by C_o given by the geometric average of C_{ox} and C_{dep}) has different slopes at the accumulation and fully-depletion region, as shown in Fig. 2(a). Because the use of fully-saturated ferroelectric hysteresis loop is desirable to guarantee the stable memory operations, the required V_{ON} and V_{OFF} of the proposed MemTFT can be estimated by the interceptions of P_s-$V_{F,sat}$ saturated hysteresis and calculated load-line, as shown in Fig. 2(b), and the following equations.

$$V_{ON} = \frac{P_S \cdot d_{ox}}{\varepsilon_0 \cdot \varepsilon_{ox}} + V_{F,sat} \quad (1)$$

$$V_{OFF} = \frac{P_s}{C_{ox}}\left(1+\frac{\varepsilon_{ox}\cdot d_s}{\varepsilon_s \cdot d_{ox}}\right) + V_{F,sat}, \quad \text{where } C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{d_{ox}}, \quad (2)$$

where P_s and $V_{F,sat}$ are saturated polarization charge density of the P(VDF-TrFE) and corresponding applied voltage. ε_{ox}, ε_s, d_{ox}, d_s are dielectric constants and film thicknesses of Al_2O_3 and ZnO layers, respectively. As can be seen in Fig. 2(b), the V_{OFF} and the depolarization field induced at 0 V for OFF state ($E_{DP,OFF}$) are larger than those (V_{ON} and $E_{DP,ON}$) for the ON state, which provides a very important insight to design the gate stack structure.

3. Fabrication of Nonvolatile Memory TFT

The fabrication procedures were carried out as follows. Firstly, source/drain (S/D) electrodes of ITO were patterned on the glass substrate. ZnO and Al_2O_3 were deposited by atomic-layer deposition at 200°C in a successive manner, in which film thicknesses of ZnO and Al_2O_3 were controlled to be from 5 to 20 nm and from 4 to 9 nm, respectively. After patterning the gate channel, P(VDF-TrFE) film was formed by spin-coating method using a 3wt% diluted solution of 70/30 mol% P(VDF-TrFE) in a dimethylformamide. The final heat treatment was performed at 140°C for its crystallization. The film thickness was approximately 80 nm. The given areas of P(VDF-TrFE) layer were removed by O_2 plasma to form the S/D contacts. Finally, Al was deposited as gate electrode and S/D pads and patterned by wet etching. Fig. 1(b) shows the photograph of the fabricated MemTFT.

4. Device Characterization & Discussions

Figs. 3(a)-3(f) show the drain current (I_D)-gate voltage (V_G) behaviors and the gate leakage currents (I_G) for the fabricated MemTFTs when the ZnO (5, 10, 20 nm) and Al_2O_3 (4 and 9 nm) thicknesses were varied. The gate width (W) and length (L) were 40 and 20 μm. All devices exhibited counterclockwise hysteretic behaviors in transfer curves, which was originated from the ferroelectric nature of P(VDF-TrFE). I_G as low as 10^{-11} A and steep subthreshold swing (about 400 mV/dec), and 7-orders-of magnitude of ON/OFF ratio are excellent performances for the NV-MemTFTs using P(VDF-TrFE). These results were realized by the introduction of thin Al_2O_3 layer.

Here, we discuss some important points related to the memory and TFT behaviors. (i) Memory window (MW), which is defined as the quantity in turn-on voltage (V_{ton}) shift, was closely related to the thickness configurations of Al_2O_3/ZnO layers. Fig. 4(a) summarizes the MW values with the same V_G sweep range (-10 V~12 V) for each device. The largest MW of 4.2 V was obtained for the TFT with 5 nm ZnO/4 nm Al_2O_3 and the MW decreased as the increase of ZnO and/or Al_2O_3 thicknesses, as expected in Fig. 2(b). (ii) The control of V_{ton} is also important. It is desirable that the MemTFT be operated in an enhancement mode for the practical applications. For the thinner ZnO channel device, the V_{ton} is generally determined at more positive range in V_G owing to its lower carrier concentration. While the devices with 9-nm-thick Al_2O_3 comply with that trend, different behaviors were observed for the case of 4-nm-thick Al_2O_3, as shown in Fig. 4(b). This suggests that the thickness of Al_2O_3 should be optimized for a sufficient MW as well as a suitable V_{ton}. (iii) The V_{ton} could be shifted to the positive direction by the post thermal annealing at 150°C for 2 h without any remarkable decrease of MW and increase of I_G, as shown in Fig. 5(a). (iv) Fig. 5(b) shows transfer curves when the channel length was varied from 40 to 5 nm, in which a clear current scaling could be observed with constant V_{ton}'s.

5. Conclusions

We fabricated and characterized the nonvolatile memory TFTs employing ZnO and P(VDF-TrFE). An important feature is that thin Al_2O_3 layer was introduced between the ZnO and P(VDF-TrFE). It was confirmed that the proper design of device parameters such as film thickness of each layer was very critical to realize better programming performances of MemTFT even with lower voltage. We can conclude from the obtained promising results that the proposed MemTFT is one of the most suitable candidates for the nonvolatile memory device embedded in the future flexible and transparent electronic applications.

Acknowledgements

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References

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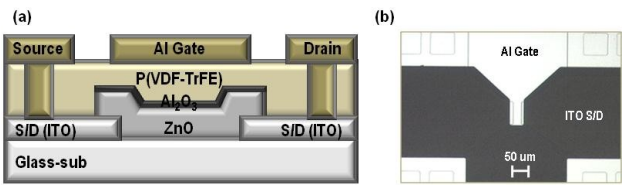

Fig. 1 (a) Cross-sectional schematic diagram and (a) photograph of the fabricated MemTFT.

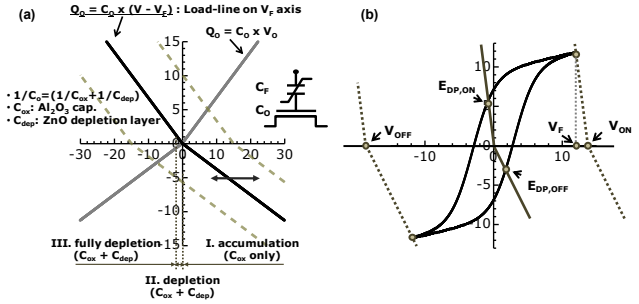

Fig. 2 (a) Load-line in Q-V plane for the determination of operating point and (b) programming voltages and depolarization fields for the proposed NV-MemTFT.

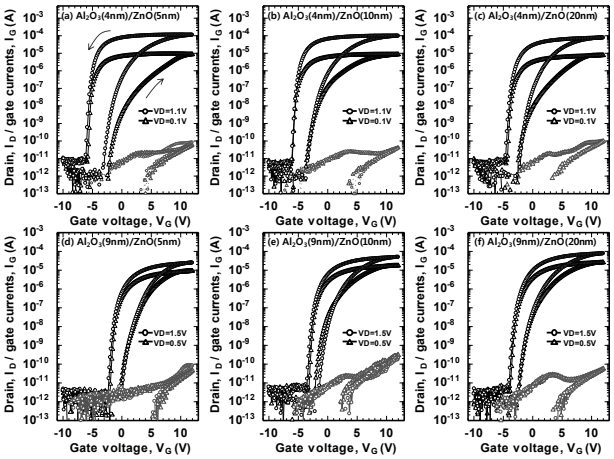

Fig. 3 Transfer curves and gate leakage currents of the MemTFTs with thickness combinations for Al_2O_3/ZnO of (a) 4/5 nm, (b) 4/10 nm, (c) 4/20 nm, (d) 9/5 nm, (e) 9/10 nm, and (f) 9/20 nm.

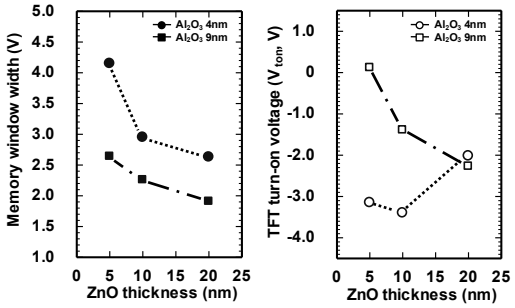

Fig. 4 Dependency of ZnO channel thickness on (a) the memory window widths and (b) turn-on voltages of each MemTFT.

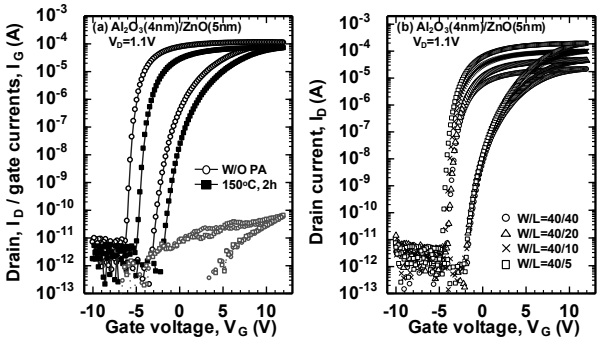

Fig. 5 (a) Post annealing process effect and (b) channel size dependency on the transfer behaviors of the MemTFT.