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# Resistance switching memory using $Si/CaF_2/CdF_2$ quantum-well structures

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## 1. Introduction

The dimension of the elements consisting integrated circuits is going down into nano-scale. One essential building block for nanoscale devices is electric potential sequences for controlling electron transport, which can be implemented using energy band discontinuity at heterointerfaces. A $CdF_2/CaF_2/Si$ heterostructure is an attractive candidate for applications on Si substrates, such as resonant tunneling diodes (RTDs)[1] and coulomb blockade devices, because of the large conduction band discontinuity ($\Delta E_C$~2.9eV) at the heterointerface [2] and small lattice mismatch with silicon. Due to the large $\Delta E_C$, leakage current is expected to be suppressed in low level even at room temperature and moreover, voltage for tunneling transport can be reduced by utilizing multi-quantum-well tunneling scheme such as resonant tunneling or sequential tunneling with appropriate design of quantum-well layer thickness sequences. Up to now, we have demonstrated large peak-to-valley current ratio (PVCR) of $CdF_2/CaF_2$ RTDs larger than $10^5$ at RT [3], which confirmed advantage of the large $\Delta E_C$. heterostructure material systems. In this paper, we have proposed and demonstrated novel scheme of resistance switching diode or resistance random access memory (ReRAM) using $Si/CaF_2/CdF_2/CaF_2/Si$ quantum-well structure. Using this architecture, resistance modulation (ON/OFF) ratio more than 1000 can be expected because of the tunneling probability variation caused by potential modulation due to electron charge/discharge in the $CdF_2$ quantum-well. In principle, low voltage write/erase and long retention time can be expected simultaneously under appropriate design because of the $Si/CaF_2$ double step energy barrier structures.

## 2. Structure

Figure1 shows schematic device structure and band diagram (flat band) proposed in this study. Basic concept of the device is $CaF_2/CdF_2/CaF_2$ double-barrier resonant tunneling diode structure or quantum-well (QW) structure sandwiched by silicon as the secondary energy barriers. $CaF_2$ layers act as energy barriers mainly for charge injection and ejection between a $CdF_2$ QW and a reservoir of electrons. Si layers act as energy barriers for suppression of electron escape from the $CdF_2$ QW. Using this layer configuration, write/erase voltage can be controlled in the range of 1 - 3 V by designing the appropriate thickness of $CdF_2$ quantum-well (2.5 nm is one example) based on resonant tunneling scheme. Injected electrons are retained in $CdF_2$ QW because conduction band minimum of $CdF_2$ is ~0.6eV lower than that of Si therefore retention time can be controlled by the thickness of Si layers. Figure 2 shows operation principle of the device. In writing operation, electrons are injected from an n-Si layer by resonant tunneling and a part of the electrons are trapped in $CdF_2$ QW as shown in (b). Trapped electrons are confined in $CdF_2$ QW by $CaF_2$ and Si energy barriers as shown in (c). In the result, resistance switching occur at around peak voltage of RTD. Resistance modulation (ON/OFF) ratio of more than 1000 can be expected theoretically due to the difference of tunneling probability between (b) and (c) under appropriate layer thickness configuration. Transmission coefficient for each mode was calculated and write and erase voltage has been evaluated based on transfer matrix method and Esaki-Tsu formula.

## 3. Fabrication

A device structure was grown in a $SiO_2$ hole of 1μm-diameter formed on Si substrate using photo lithography and wet etching. Firstly, a 1.6-nm-thick $CaF_2$ layer was grown at 650°C by molecular beam epitaxy (MBE) based technique. Subsequently, a 2.5-nm-thick $CdF_2$ quantum-well layer, 0.9-nm-thick $CaF_2$ layer, and a Si barrier layer (0.6-3nm-thick) were grown at 80°C. After unloaded from the UHV chamber, Al/Au electrodes were formed by lift-off.

## 4. Results and discussions

In the measurement of I-V curve shown in Fig. 3, resistance switching has been clearly observed at room temperature, where switching voltage (low resistance state to high resistance state) was 2.4 V ("write" voltage), peak current density was 1.6 $A/cm^2$ and peak-to-valley current ratio was around 100. Voltage for discharge or "erase" operation was found to be -3V. Switching voltage can be controlled and reduced by optimization of the thickness of $CdF_2$ quantum-well. Peak current density can be increased by reducing thickness of $CaF_2$ barrier layers.

## 5. Conclusion

We have proposed and demonstrated novel resistance switching diode using $Si/CaF_2/CdF_2$ double step tunneling barriers and one quantum-well structure. Resistance switching memory operation has been clearly observed at room temperature. Device concept proposed in this study is one possible candidate for new volatile memories or logic elements for future LSI technologies toward ultimate scaling

in nanometer scale.

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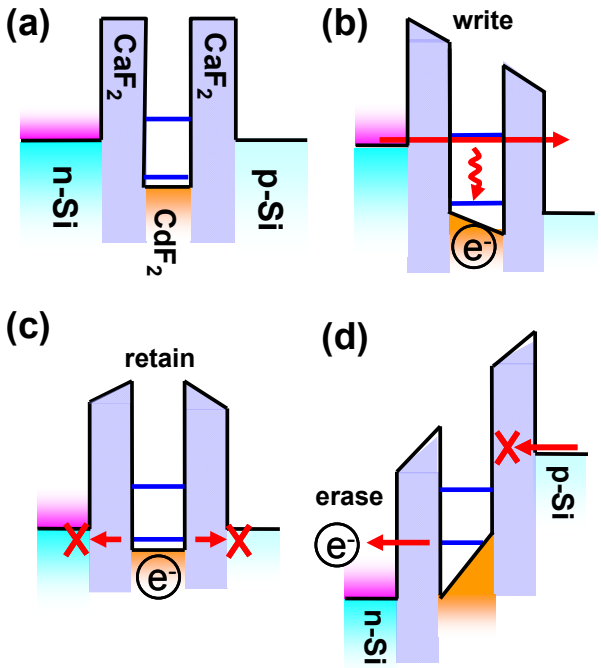


Fig.2 Band diagrams corresponding to (a) flat band potential, (b) "write", (c) "retain", (d) "erase" operation.

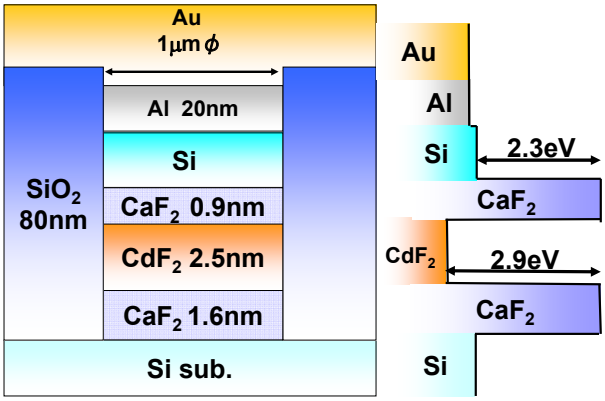


Fig.1 Schematic device structure and conduction band profile.

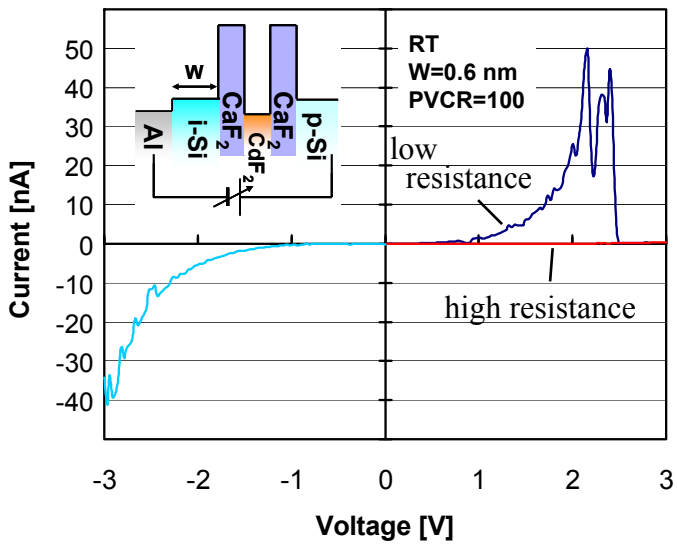


Fig.3 I-V curve at RT exhibiting resistance switching. Switching voltage can be controlled by changing thickness of $CdF_2$ quantum-well.