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Self-aligned Metal Double-gate P-channel Low-temperature Poly-Si TFTs Fabricated by DPSS CW Green Laser Lateral Crystallization

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Abstract

Self-aligned top and bottom metal double-gate (DG) p-channel (p-ch) low-temperature (LT) polycrystalline silicon (poly-Si) thin-film transistors (TFTs) were fabricated at 550°C. High-quality Si thin film, which was fabricated by diode-pumped solid-state (DPSS) continuous wave (CW) green laser lateral crystallization, was used as the channel layer. It was observed that the on-current of the TFTs was nearly double that of the top-gate (TG) p-ch LT poly-Si TFTs, and the S-value of the former was smaller than that of the latter.

Introduction

The multigate structure is considered to be the main candidate for realizing ideal Si transistors in the nano-CMOS era. This technique also leads to the improvement of the performance of poly-Si TFTs. High-quality poly-Si films are important for improving the performance of poly-Si TFTs. DPSS CW green laser crystallization is an excellent technique that can be used to fabricate large-grained poly-Si films, and one of the present authors (A.H.) has succeeded in realizing high-performance TG poly-Si TFTs on non-alkali glass substrates at 450 °C using this technique.[1–3]

To fabricate LT poly-Si TFTs, particularly at temperatures below 600°C, the use of a metal gate is necessary. In the present study, we successfully fabricate self-aligned top and bottom metal DG p-ch LT poly-Si TFTs with large-grained poly-Si film that show good performance.

Experiments

Figure 1 shows a three-dimensional image of the TFTs during fabrication and an optical photograph of the actual devices after the completion of several key processes. Fused quartz glass was used in this experiment. After a bottom Mo gate was patterned (Figs. 1(a) and (a′)), a SiO_2 layer and a a-Si layer were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 325°C using SiH_4 + N_2O for the SiO_2 deposition and SiH_4 + H_2 for the a-Si deposition. After dehydrogenation annealing at 500°C for 60 min in N_2 gas, a-Si was crystallized by using a stable scanning DPSS CW green laser (λ = 532 nm, 2ω of Nd:YVO_4) with a speed of 40 cm/s. The laser spot size in this experiment was set at 400 × 20 μm^2 using two cylindrical lenses. The power instability of the DPSS CW green laser was less than 1%, which is less than the values in the case of XeCl excimer and Ar lasers. After Si-island formation by dry etching, the top SiO_2 gate layer was deposited by PECVD (Figs. 1(b) and (b′)). Subsequently, the contact hole for connecting the top and bottom metal gates was formed by dry etching. After slight etching using a diluted HF solution to remove the oxidized layer on the surface of the bottom Mo gate, sputtered Mo was deposited. To form a self-aligned top Mo gate, back-surface exposure of the g-line was performed by using the bottom Mo gate as a mask. The film thickness of the top Mo gate was sufficiently small (30 nm) for the film to be transparent to g-line light. On the other hand, the bottom Mo gate was sufficiently thick (50 nm) for the film to act as a metal mask in the formation of the self-aligned top gate by back-surface exposure. After the wet etching of the sputtered top Mo metal, the self-aligned top Mo gate was fabricated (Figs. 1(c) and (c′)). After the removal of the SiO_2 layer on the source and drain regions by dry etching, ion implantation of BF_2 was performed with an acceleration energy of 20 keV and an ion dose of 3 × 10^{15} cm^{-2}. After annealing at 550°C for 6 h for activation, a SiO_2 isolation layer and a Mo electrode were formed by PECVD and sputtering, respectively.

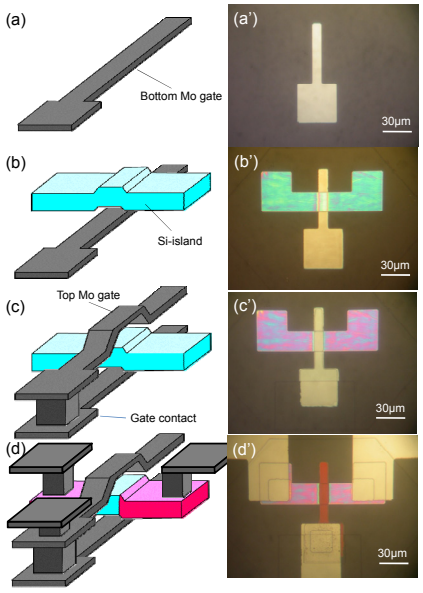

Fig. 1. Three-dimensional images of poly-Si TFTs after the completion of key processes. The photographs to the right show the top view of an actual device after the processes.

Figure 1(d′) shows a photograph of the top view of a metal DG p-ch LT poly-Si TFT. The active Si channel layer is undoped and is 100-nm thick. The top and bottom SiO_2 gate layers are designed to be 50-nm thick. The maximum temperature in the poly-Si fabrication process was 550°C. Fused quartz glass was used in this experiment. It is well known that the DPSS CW green laser can be used for the crystallization of Si film on a non-alkali glass substrate;[1–3] thus, the technique developed in this experiment can easily be applied to non-alkali glass substrates.

Results and discussions

Figure 1(b′) shows an optical microscope image of a poly-Si island on the bottom Mo gate. The crystallized poly-Si film is composed of very large grains, which are generally parallel to one another and in the scan direction of the laser beam. The surface of the crystallized poly-Si film is very smooth, and the grain boundaries do not form ridges. Figure 2 shows Raman scattering spectra of the poly-Si film

on the bottom Mo gate. The full width at half maximum (FWHM) of the micro-Raman scattering spectra is 4.3 cm^{-1}, which is close to that in the case of Si wafer (4.1 cm^{-1}). The crystallization method used in this experiment facilitates the easy formation of large grains for a wide range of laser beam energies when the laser scan speed is high. Laser scanning leads to the development of a temperature gradient at the solid-liquid interface, and the temperatures in the front molten-Si region and the rear solid-Si region are high and low, respectively. This temperature gradient stabilizes the crystallization process.

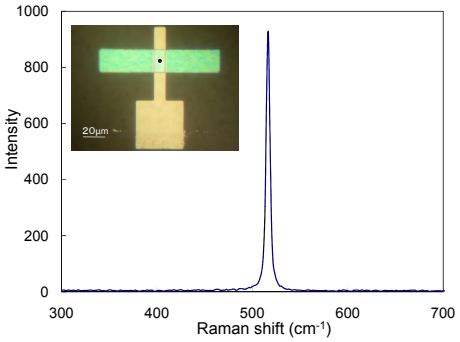

Fig. 2. Raman scattering spectra of Si in the black dot region in the inset.

Figure 3 shows a comparison between the transfer and output characteristics of DG TFTs and those of TG p-ch LT poly-Si TFTs. The gate length and width in the case of both TFTs are 20 μm. A small S-value of 200 mV/dec and a large on/off current that is greater than 10^6 are observed in the case of the DG LT poly-Si TFTs, while the S-value is 290 mV/dec for the TG LT poly-Si TFTs, as shown in Fig. 3(a). Figure 3(b) shows the output characteristics of the DG p-ch LT poly-Si TFTs and TG p-ch LT poly-Si TFTs. The on-current of the former is double that of the latter. These superior characteristics of DG p-ch LT poly-Si TFTs are direct evidence of the double-gate operation.

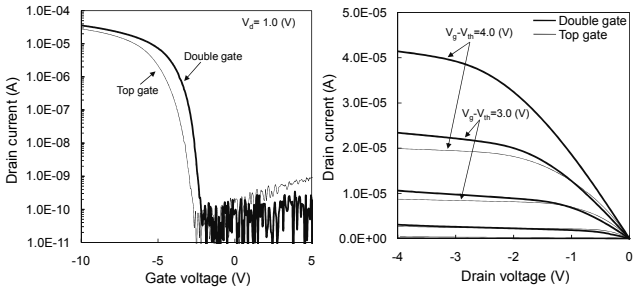

Fig.3. (a) The transfer characteristics of self-aligned DG p-ch LT poly-Si TFTs and TG p-ch LT poly-Si TFTs. (b) Output characteristics. Gate length and gate width of both TFTs are 20 μm. Top and bottom gate SiO_2 thicknesses for the DG poly-Si TFTs are 50 nm. Gate SiO_2 of the TG poly-Si TFTs is 50 nm thick.

The nominal field-effect mobilities of DG p-ch LT poly-Si TFTs and TG p-ch LT poly-Si TFTs, as calculated from the linear region, are 90 and 48 cm^2/Vs, respectively. These values are much smaller than those obtained for TG p-ch LT poly-Si TFTs in previous studies.[1–3] Figure 4 shows the variation of the on-current with the gate length under same bias condition. It is observed that the on-current shows a saturation tendency with a decrease in the gate length. This tendency indicates that the S/D regions and contact regions have a high parasitic resistance. In previous studies, excimer laser activation has been used for S/D activation; in contrast, low-temperature thermal activation is used in this experiment. To improve the on-current, preamorphization of the S/D region by Ge implantation prior to dopant implantation seems to be a good approach; this approach has been proposed in ref.[4]

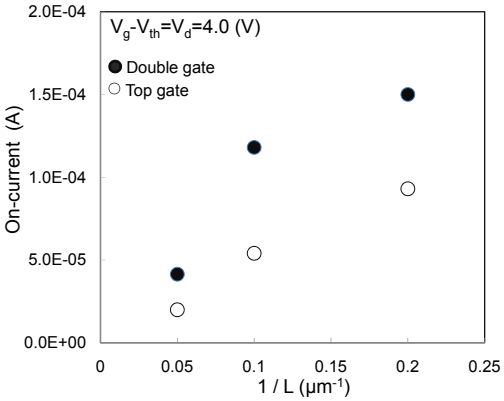

Fig. 4. Dependence of on-current on gate length.

The value of V_{th} for this TFT is –2.5 V. In the experiment performed in the present study, the channel region is undoped. V_{th} can be improved by doping the channel and using other gate metals, which would have different work functions.

One of the present authors (A.H.) had fabricated self-aligned metal DG n-ch LT poly-Si TFTs and had confirmed their good performance.[5] The results of this experiment may contribute to the production of high-speed, low-power-consuming CMOS poly-Si TFT circuits on glass substrates.

Summary

Self-aligned metal DG p-ch LT poly-Si TFTs were fabricated at 550°C by DPSS CW green laser lateral crystallization. It was observed that the on-current of the TFTs was nearly double that of the TG p-ch LT poly-Si TFTs. A small S-value of 200 mV/dec and a large on/off ratio greater than 10^6 were obtained for a gate SiO_2 thickness of 50 nm. One of the present authors (A.H.) had previously fabricated self-aligned metal DG n-ch LT poly-Si TFTs and had confirmed that their performance was very good. The results of this experiment are expected to contribute to the production of high-speed, low-power-consuming CMOS poly-Si TFT circuits on glass substrates.

Acknowledgement

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