Electromechanical Systems for Memory and Logic Devices

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More than 150 years ago Charles Babbage conceived the idea of a programmable computer. Babbage developed his analytical engine in a mechanical architecture where logic was performed by moving parts. In the microelectronics age these ground breaking ideas were forgotten as silicon transistor technology was the system of choice for implementing logic. We demonstrate that in the era of nanotechnology the mechanical computer can be revived and logic can be implemented by electromechanical systems.

The Parametron is a logic processing system first developed 50 years ago. It utilises the parametrically excited resonance of a harmonic oscillator, where this oscillation has two stable phases separated by π radians, as the basis for logic operations. The computational architecture based on this principle was well developed using an LC oscillator but was rendered obsolete by the transistor due to its high power consumption and integration difficulties in dense system architectures. To remedy these drawbacks, we propose to implement mechanical logic in the mould of the Parametron with electromechanical systems.

In the first steps to this goal, we demonstrate both bit storage and bit flip operations in an electromechanical oscillator. We do this by integrating a two dimensional electron system (2DES) into the mechanical oscillator which enables electromechanical transduction via the piezoelectric effect. This enables on-chip all electrical actuation of the parametric resonance and detection of the fundamental mode as well as switching between the two phases of oscillation i.e. all the necessary prerequisites for the electromechanical Parametron computer. The electromechanical bit operation demonstrated here paves the way for realising a nanomechanical computer.

The electromechanical oscillator was realised from a GaAs/AlGaAs heterostructure and is shown in Fig.1. A parametric resonance could be excited by modulating the spring constant of the oscillator at twice its natural frequency via the piezoelectric effect between the top-gate and the 2DES. The parametric resonance line shape shown in Fig. 2 is highly asymmetric as the parametric resonator can oscillate with two stable phases (0 and π) separated by π radian in region (ii) whereas as in region (iii) the stationary state of the parametric resonator also becomes available.

![Figure 1: A simplified schematic of the electromechanical resonator showing the III-V semiconductor sandwiched between the Au top-gate and the 2DES at both clamping points. Application of voltage across this sandwich structure results in the transduction of the parametric resonance via the piezoelectric effect. Also shown is the exaggerated out-of-plane flexural mode where typical amplitudes were of the nm order. A false colour SEM image shows the intricate gate structure used in the real devices.](image)

Using this parametric bi-stability (i.e. region (ii) in Fig. 2), binary data storage can realised by assigning binary states “0” and “1” to the 0 and π oscillation phases as in the original Parametron computer.
In Fig. 3, the “0” and “1” bit states are periodically stored in the phase of the parametric resonance at various clock frequencies $f_c$.

![Graph showing parametric resonance phases](image)

Figure 2: The parametric resonance excited via the largest gate and detected by one of the smaller gates (shown in Fig. 1) in a high vacuum at 2.5 K. The red and black traces correspond to increasing and decreasing the actuation frequency across the resonance respectively. The solid and dotted lines correspond to the 0 and $\pi$ oscillation phases where the parametric resonance phase information is encoded in either the real or imaginary part of the measured signal. Mechanical logic can be implemented in region (ii) i.e. where the parametric resonance is bi-stable.

By combining multiple mechanical parametric resonators, shift registers and AND/OR logic gates can be constructed i.e. the necessary precursors for a mechanical computer. A shift register can be realised by simply connecting the output electrode of a mechanical bit to the input electrode of the next mechanical bit. Binary information can be transmitted when the phase of the parametric resonance of the next mechanical bit is triggered by the output of the previous mechanical bit. AND/OR logic gates can be implemented by utilising the majority voter concept. In this case, the output electrodes from three mechanical bits are connected to the input of a fourth mechanical bit. The parametric resonance output of the three mechanical bits are superimposed and the resultant phase is then injected into the fourth mechanical bit enabling AND/OR logic operations to be implemented.

![Graph showing bit-storage and bit-flip protocol](image)

Figure 3: The bit-storage and the bit-flip protocol where “0” and “1” bit states are periodically stored in the 0 and $\pi$ oscillations phases respectively by triggering the appropriate oscillation phase with smallest top-gate at $f_c = 0.01$ Hz (a) and 0.03 Hz (b). The system is reset by simply deactivating the parametric resonance i.e. 0 V in the above figures.

The natural frequency of the electromechanical resonator can exceed 1 GHz by simply minimising the dimensions of the oscillator enabling high speed logic to be realised. Moreover, the energy consumption in such small mechanical resonators will be extremely small ($\ll$ pJ/bit). Thus, memory and logic devices based on such mechanical oscillators are highly attractive as they could offer a route towards a new generation of ultra energy efficient computers.

References


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