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Electrical control of the magnetic properties in (Ga,Mn)As channel in electric double layer transistor

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1. Introduction

A III-V based ferromagnetic semiconductor (Ga,Mn)As is regarded as one of the candidate materials for new spintronics devices [1,2]. Ferromagnetic order of (Ga,Mn)As is brought about by exchange coupling between Mn spins and holes provided by Mn acceptors substituting Ga sites. Thus, one can control the magnetic properties, such as the Curie temperature T_C, magnetic anisotropy H_A, and coercivity H_C of a (Ga,Mn)As channel in metal-insulator-semiconductor field-effect transistor (MISFET) structure by applying electric-fields [3-7]. For a larger modulation of the magnetic properties, higher modulation of hole concentration p is needed. In MISFET, the modulation of p is proportional to gate electric-fields $E_G = V_G/ d_{ins}$, where V_G is gate voltage and d_{ins} is insulator thickness. In electric double layer transistor (EDLT) [8], it is possible to apply electric-fields exceeding 10 MV/cm by applying a few volts of gate voltage, because the electric double layer, which is a capacitor with a few nanoscale thickness, is formed at the interface between the semiconductor and the polymer electrolyte (Fig. 1). In this work, we have fabricated (Ga,Mn)As EDLT and investigated the electrical control of conductance and magnetic properties.

2. Sample growth and device fabrication

A $Ga_{0.948}Mn_{0.052}As$ with thickness t = 4.5 nm was grown on a semi-insulating GaAs (001) substrate with an underneath buffer of 4 nm GaAs / 30 nm $Al_{0.74}Ga_{0.26}As$ / 500 nm $In_{0.15}Ga_{0.85}As$ / 30 nm GaAs by molecular beam epitaxy (MBE). The sample was annealed for 40 min at 180 ^{o}C in air and processed into a mesa with width of 30 μm and length of 100 μm, by photolithography and wet etching. Subsequently, Au/Cr electrode pads were evaporated and lifted-off for source and drain contacts, gate electrode, and voltage probes to measure the sheet and Hall resistances. The gate has a large enough area to apply most of the gate voltage to (Ga,Mn)As channel. We bonded Au wires to electrodes and covered all the area except for the channel region and gate electrode by silicone adhesive sealant [9]. Finally, we dropped the polymer electrolyte, which is composed a mixture of $KClO_4$ ([O]/[K] = 30) and poly-ethylene-oxide (M_w = 2000), on channel and gate electrode [9-11]. The electrolyte was heated at 90^{o}C for more than an hour in vacuum in order to dehydrate before dropping, and then cooled down to ~10^{o}C to solidify after dropping.

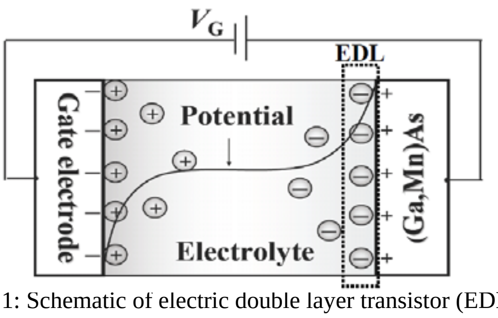

Fig. 1: Schematic of electric double layer transistor (EDLT). EDL is formed at the interface between (Ga,Mn)As and polymer electrolyte.

3. Results

In order to investigate the magnetic properties under a gate voltage in (Ga,Mn)As EDLT, we have measured the magnetic field H dependence of the Hall resistance R_{Hall} as a function of temperature at V_G = 0 (Fig. 2 (a)). In general, the Hall resistance R_{Hall} in magnetic materials can be expressed as follows,

$$R_{\mathrm{Hall}} = \frac{R_0}{t}\mu_0 H + \frac{R_s}{t} M \quad \cdots \quad (1)$$

, where R_0 is the ordinary Hall coefficient, R_S is the anomalous Hall coefficient, μ_0 is permeability in vacuum, and M is the perpendicular component of magnetization in the (Ga,Mn)As channel layer. R_{Hall} is nearly proportional to M below and around T_C, where the anomalous Hall effect is dominant. The R_{Hall} - $\mu_0 H$ curves in Fig. 2(a) show square hysteresis loops indicating a ferromagnetic order in (Ga,Mn)As at low temperatures. We measured the Hall resistance under three difference gate voltages (V_G = -4, 0, and 4 V) at 60 K (Fig. 2(b)). The application of negative

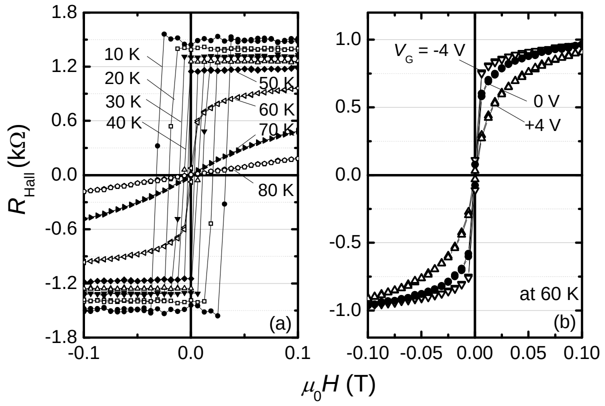

Fig. 2: The magnetic field dependence of Hall resistance R_{Hall} as a function of (a) temperature and (b) gate voltage at 60 K.

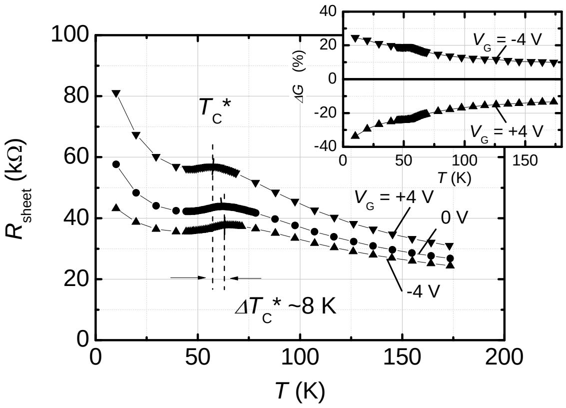

Fig. 3: The temperature dependence of sheet resistance R_{sheet} under three different gate voltages. T_C* is the temperature at which hump appears. Inset shows the temperature dependence of the modulation ratio of sheet conductance.

gate voltage enhanced, whereas positive one suppressed ferromagnetic order, which is consistent with the previous works.

We have measured also the temperature dependence of sheet resistance R_{sheet} under several V_G (Fig. 3). One can see that R_{sheet} increases by the application of V_G = +4 V, whereas that decreases by the application of V_G = -4 V. Inset in Fig. 3 indicates the temperature dependence of modulation ratio of sheet conductance G (= $1/R_{sheet}$), which is determined by $\Delta G = (G(V_G)-G(0))/G(0)$. ΔG is changed more than 10 (-10)% by applying V_G = -4 (+4) V and increases as decreasing temperature, which is occurred by the reduction of hole concentration due to week localization.

R_{sheet} increases as temperature decreases and one can see the hump, which appears in the vicinity of T_C in (Ga,Mn)As, around 60 K in all the curves [12]. We refer the hump temperature to T_C*. T_C* is 56 K at V_G = +4 V, and is 64 K at V_G = -4 V. The change of T_C*, ΔT_C* = 8 K with ΔV_G = 8 V is ten-times larger modulation ratio than that of (Ga,Mn)As MISFET with a solid insulators such as Al_2O_3 because latter needs larger than a few tens of volts.

4. Conclusions

In conclusion, we have demonstrated the change of magnetic and transport properties in (Ga,Mn)As by applying a few volts to the gate by utilizing the EDLT structure. We can change the T_C by 8 K and sheet conductance G by 20% by changing the gate voltage from -4 V to +4 V. This capacitance structure will be useful for investigation of physics in ferromagnetic semiconductors and their device application in the future.

Acknowledgements

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