Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1394-1395

The Performance of Magnetic Tunnel Junction Integrated on the Back-end Metal Line of CMOS Circuits

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1. Introduction

Recently, new applications using Magnetic Tunnel Junction (MTJ)-based logic, where nonvolatile storage elements are distributed over a CMOS logic-circuit plane, has been studied [1-3]. However, the fabrication of high-performance MTJs on CMOS circuits has not been straightforward because of the roughness of the CMOS circuit plane. MTJs integrated in CMOS circuits must satisfy the following three points: (1) MTJ must be write by a standard MOSFET with low power consumption, and (2) resistance of MTJ and the Tunnel Magneto-Resistance (TMR) ratio must be large enough for the sensing scheme of a standard CMOS logic. Here, TMR ratio is defined as $(R_{AP}-R_P)/R_P$, where high resistance R_{AP} and low resistance R_P are the resistance at anti-parallel (AP) and parallel (P) configurations of the free and fixed layers, respectively. (3) The size of an MTJ must be small for scaling and low-power consumption.

In this paper, the CMOS/MTJ integrated process technology with 0.14 μm CMOS and 60x180nm^2 MTJ is described, and it is shown that the fabricated MTJ integrated on CMOS achieve excellent Write/Read performance for realizing MTJ-based logic.

2. Fabrication of CMOS/MTJ integrated IC

We fabricated MTJ on a CMOS logic-circuit plane with 4-Metal / 1-poly gate 0.14 μm CMOS process technology. Figure 1 shows the fabricated MTJ integrated in CMOS circuits. MTJs were stacked on via metal of the 3rd metal layer with surface roughness of less than 0.3nm planarized by CMP. The MTJ stack consists of $Co_{20}Fe_{60}B_{20}$(2)/ Ru(0.8)/$Co_{20}Fe_{60}B_{20}$(1.8) synthetic ferrimagnetic (SyF) free-layer, a 1-nm-thick MgO tunnel barrier, and a $Co_{20}Fe_{60}B_{20}$ fixed-layer. The annealing temperature is 325°C. After MTJ stack is deposited, junction of 60x180nm^2 and top metal line over MTJs are fabricated by using electron beam lithography and ion milling.

3. Performance of MTJ integrated on CMOS

In order to evaluate the performance of MTJ with Current Induced Magnetization Switching (CIMS), the DC and AC characteristics were measured. All measurements were performed at room temperature and without a magnetic field. R-I characteristic of the MTJ integrated in CMOS circuits, as shown in Fig.2, shows the switching of magnetization by only current and hysteresis curve of the MTJ. TMR ratio of 138% is achieved with R_{AP} of 3.63kΩ and R_P of 1.53kΩ. I-V characteristic is measured as shown in Fig.3 and the normalized TMR ratio and output voltage ($\Delta V = V \times (R_{AP}-R_P)/R_P$) are plotted in Fig.4 as a function of bias voltage of V. Output voltage of ΔV of over 500mV is reached. In order to evaluate the critical current density of J_c, resistance versus pulsed current density (R-J) curves from τ_p = 500μs to 0.1s were measured. In R-J curve [shown in Fig.5 for τ_p= 1ms], a switching is observed at a critical current density of J_c. By extrapolation of J_c measured at several different τ_p to $\ln(\tau_p/\tau_0)$ of 0 as shown in Fig.6, where τ_0 = 1ns corresponds to the ferromagnetic resonance time constant of the free layer, we obtain J_{c0}^{ave} [= ($|J_{c0}^{P->AP}| + |J_{c0}^{AP->P}|$) / 2] of 7.7x10^{6}A/cm^2.

The write current density of 7.7x10^{6}A/cm^2 can be driven by a standard MOS transistor, as drive current per gate width is typically 1mA/1μm and size of fabricated MTJ is 60x180nm^2. R_{AP} of 3.63kΩ is large enough in comparison with channel resistance of a MOS transistor of 200Ω/1μm channel length. Furthermore, since the TMR ratio of 138% is relatively high, good read margin would be obtained. The MTJ size of 60x180 nm^2 is comparable to the employed CMOS technology. Above all, our MTJ integrated in CMOS circuits has high enough performance to construct MTJ-based logic with CMOS circuit.

4. MTJ operation with CMOS circuit

We demonstrate the DC and AC operation of this MTJ with write transistors. Figure 7 shows the photograph of the fabricated MTJ with two write transistors. The pulse current is generated by these MOSFETs. The write pulse voltage applying to both Gate1 and Gate2 and the bias voltage between WD and WS are set to 1.5V and 1.0V, respectively, where WD, WS, Gate1 and Gate2 are shown in the inset of Fig.7. Figure 8 shows the measured current flowing between WD and WS, and the write pulse voltage. As shown in Fig.8, after 230ns when the write pulse is applied to Gate1/Gate2, current through the MTJ changed from 550μA to 750μA. At this timing, magnetization configuration changed from anti-parallel(AP) to parallel(P) by CIMS. Which demonstrate that the fabricated MTJs integrated on CMOS logic have excellent Write/Read performance.

5. Conclusions

In this paper, we have described the CMOS/MTJ integrated process technology; MTJs were fabricated on via metal with surface roughness of 0.3nm with 0.14μm CMOS process and 60x180nm^2 MTJ process, as summarized in Table 1. It is shown that the fabricated MTJ integrated on CMOS achieves enoughly Write/Read performance for realizing MTJ-based logic, as summarized in Table 2.

Acknowledgements

This work was supported by Research and Development for Next-Generation Information Technology by the Ministry of

Education, Culture, Sports, Science and Technology of Japan. The authors wish to thank Kenchi Ito of Hitachi, Japan, for help in fabrication of chip and discussion.

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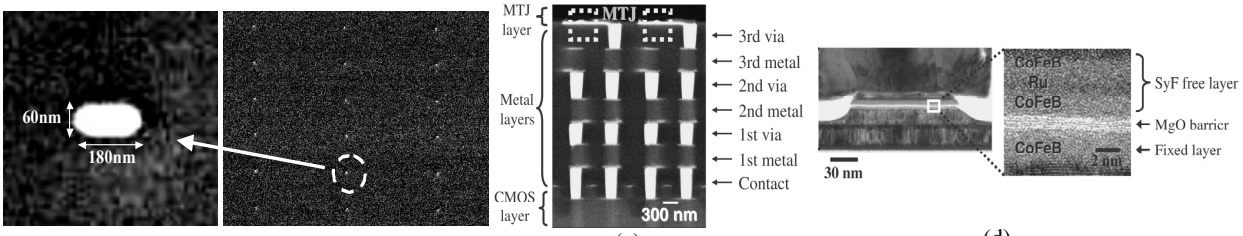

Fig. 1 Fabricated MTJ: (a) SEM image of a MTJ resist pattern of 60x180nm^2 (b) SEM image of a MTJ resist pattern array (c) Cross-sectional SEM image of the MOS transistors, metal wires which are fabricated with 0.14μm CMOS process and MTJs which are stacked over the 3rd metal layer [2] (d) Cross-sectional TEM image of MgO barrier MTJ with CoFeB/Ru/CoFeB SyF free layer [1]

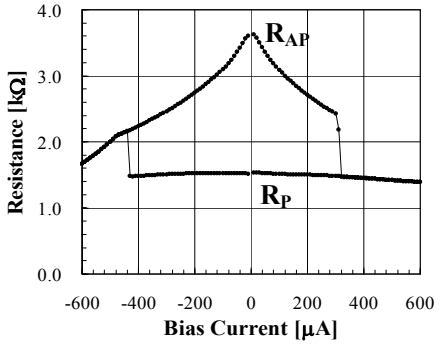

Fig.2 R-I characteristic of the MTJ integrated on CMOS. R_P and TMR ratio are 1.53kΩ, 138% respectively.

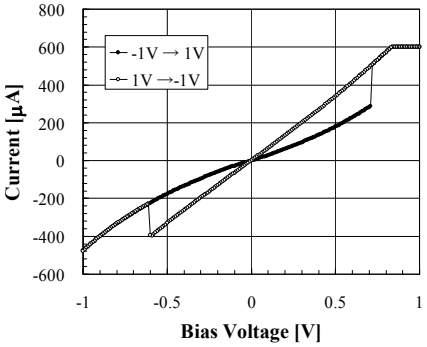

Fig.3 I-V characteristic. The MTJ can be switched by bias voltage of +0.7V/-0.6V.

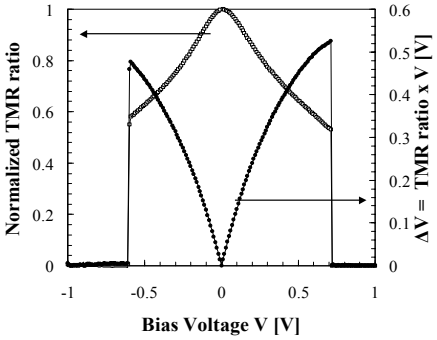

Fig.4 Bias voltage dependence of output voltage ΔV.

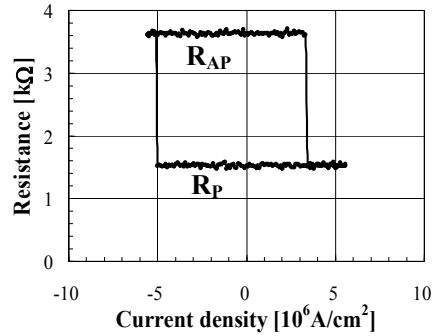

Fig.5 Resistance versus pulsed current density loop at τ_p = 1ms.

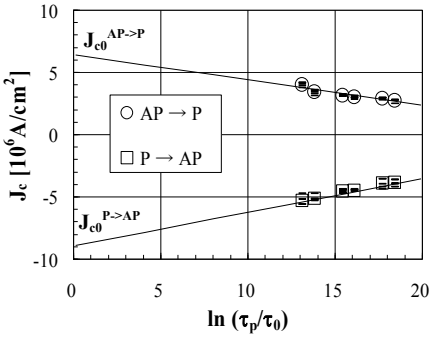

Fig.6 Critical current density J_c as function of $\ln(\tau_p/\tau_0)$. R-J measurements were performed five times.

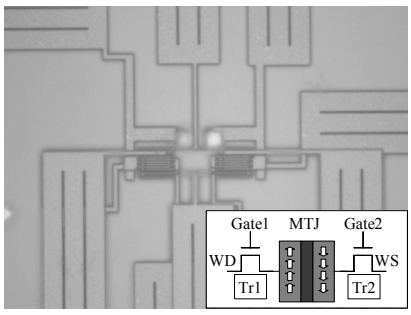

Fig.7 Photograph of CMOS/MTJ integrated IC constructed with MTJ and write transistors.

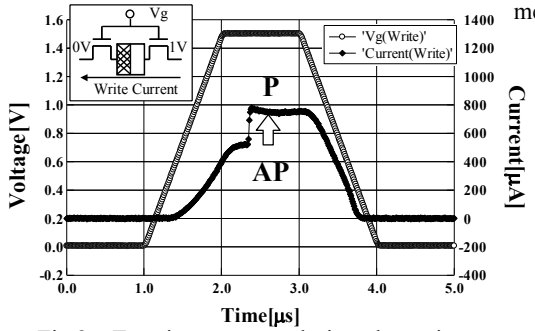

Fig.8 Transient current during the write operation. Switching from AP to P is successfully demonstrated. Write current is driven by the write transistors.

Table 1 Device Process and Structure.

CMOS Process	Front-End	0.14 μm, 1-poly gate
	Back-End	4-metal
MTJ Process	MTJ size	60nm×180nm
	Free Layer	$Co_{20}Fe_{60}B_{20}$/Ru/$Co_{20}Fe_{60}B_{20}$
	Tunnel Barrier	MgO
	Fixed Layer	$Co_{20}Fe_{60}B_{20}$
	Annealing Temperature	325°C

Table 2 MTJ Features.

Parameter	Value
TMR ratio	138%
R_{AP}	3.63 kΩ
R_P	1.53 kΩ
J_{c0}^{ave}	7.7 x10^{6}A/cm^2
$\lvert J_{c0}^{AP->P}\rvert$	6.5 x10^{6}A/cm^2
$\lvert J_{c0}^{P->AP}\rvert$	9.0 x10^{6}A/cm^2
E/k_BT	32
ΔV	500 mV