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# High-speed Magnetic Memory based on Spin-Torque Domain Wall Motion

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## 1. Introduction

Magnetoresistive random access memories (MRAMs) have unique attributes that are not found in any other memories, such as non-volatility, high-speed operation, unlimited read-write endurance, and high-temperature operation. Therefore, they have great potential as non-volatile working memories, which are predicted to replace volatile working memories such as SRAMs and DRAMs.

The positioning of conventional memory technologies is shown in Fig. 1. The horizontal axis represents the cell area factor, corresponding to chip cost, and the vertical axis represents the operating frequency, corresponding to performance. There is a tradeoff between chip cost and performance. First-generation MRAMs, which have already been commercialized, are positioned in the middle of these memory technologies and are placed slightly lower than DRAMs and SRAMs, as shown in Fig. 1. This positioning limits the expansion of MRAM applications and markets, so both higher-speed embedding and larger capacities are essential for next generation MRAMs.

This paper describes new MRAM-cell technology suitable for high-speed memory macros embedded in SoCs.

## 2. MRAM cell for embedded applications

We have developed circuit structures for high-speed operation of MRAM [1] and developed 250 MHz [2] and 32 Mb [3] memory macros. The cell consists of two pass transistors and one MTJ overlying a write line connected to both transistors. The key challenge to overcome in order to replace conventional memories such as eSRAM and eDRAM is reducing the write-current of the memory cell. We previously proposed, as a scalable cell technology, a current-induced magnetic domain wall (DW) motion MRAM using an in-plane magnetic anisotropy (IMA) free layer [4]; however the write-current had to be further reduced.

To reduce the write-current of DW-motion MRAM, we used a perpendicular magnetic anisotropy (PMA) material for the free layer. Compared with IMA materials, PMA material enables more efficient DW-motion (Fig. 3) [5]. As a result, even in a much larger critical field, the critical current density becomes one order of magnitude smaller. In addition, the DW-motion speed is expected to be ~ 50 m/s, an acceptable value for high-speed operation.

Figure 2 depicts a DW-motion cell structure with PMA films. The free layer consists of three regions: two fixed regions, the magnetizations of which are aligned anti-parallel by pinning layers, and one free region, in which DW moves during writing. Reading is performed with a magnetic tunnel junction (MTJ) composed of a reference layer, tunnel barrier, and the free region.

We used Co/Ni laminated film as the free layer and Co/Pt laminated film or Co-Pt alloy film as the pinning and reference layers. We found the Co/Ni film to be suitable for the DW-motion layer, probably due to its high spin polarization [6].

## 3. Results and Discussion

*A. Cell element performances*

Cell elements that have various widths and critical fields have been fabricated. Figure 4 shows the measured critical current as a function of free layer width. The critical current decreases as the width decreases and reaches less than 0.2 mA below 100 nm width. Such a small current enables us to achieve the smallest cell layout.

Figure 5 (a) shows measured critical current and critical field for a number of samples, and (b) shows estimated energy barrier ($\Delta E/k_BT$) by measuring self-distribution of the critical field. In agreement with a micromagnetic simulation [6], the critical current density is insensitive to the critical field, although the energy barrier increases monotonically with the critical field. These results suggest that we can reduce the write-current by scaling, with maintaining a sufficient thermal stability by forming appropriate pinning sites. This is a unique advantage of DW-motion MRAM.

Figure 6 shows the switching probabilities as a function of voltage for different pulse durations. DW velocity is estimated to be more than 50 m/s, corresponding to 3 ns switching for DW-motion length $\ell$ of 200 nm. This suggests that writing within 2 ns is possible for $\ell \sim 100$ nm.

*B. Memory Operations*

Figure 7 shows 4k-bit arrays with decoder circuits that have been fabricated. Figure 8 shows a resistance histogram after +I and –I currents had been injected into the array device. R0 and R1 are clearly separated. Figure 9 shows R-I properties for DW-motion cell for the array. In Fig. 9, MR ratio was about 40%, which was increased up to 100% by a change in magnetic layer composition. Figure 10 shows repeat test results. Good reproducible switching and overwrite properties were achieved.

## 4. Conclusion

We have successfully developed a new magnetic random access memory with current-induced domain wall motion. We confirmed its potentials of less than 0.2 mA and 2 ns writing with sufficient thermal stability. The obtained properties indicate that this MRAM can replace conventional high-speed embedded memories.

**Acknowledgements**

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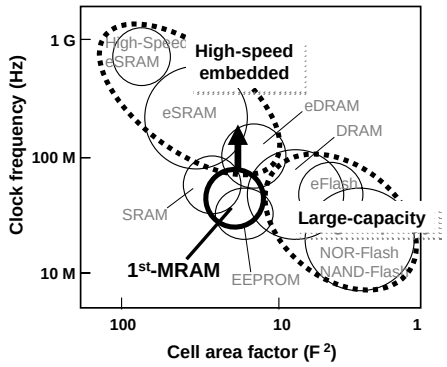


Fig. 1. Positioning for semiconductor memories. The horizontal axis represents the cell area factor, and the vertical axis represents the operating frequency.

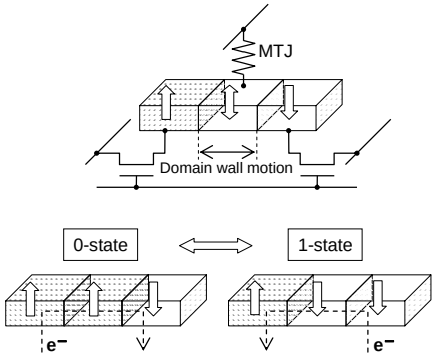


Fig. 2. Structure of cell with domain wall motion. A single DW was introduced in to and trapped in the end of the middle part and was moved by spin-polarized electrons.

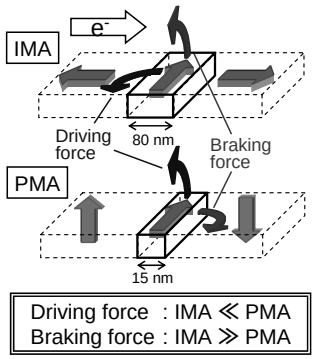


Fig. 3. Difference between in-plane (IMA) and perpendicular magnetic anisotropy (PMA). PMA shows large driving force and small braking force.

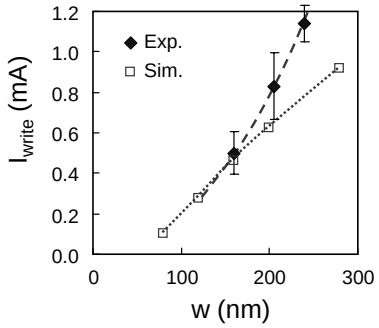


Fig. 4. Critical current as a function of free layer width. Write current reaches to 0.1 mA at w < 100 nm.

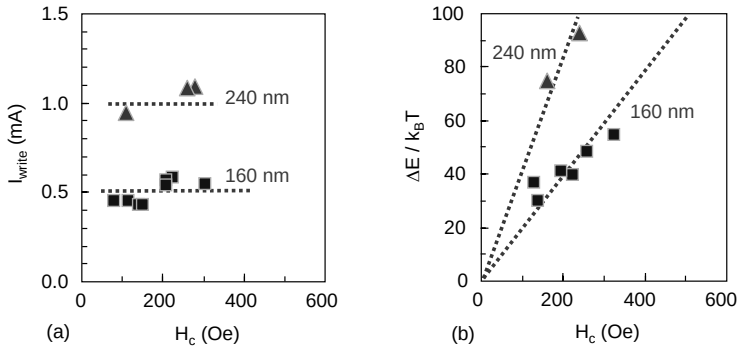


Fig. 5. (a) Critical current and (b) energy barrier for a number of samples that have different critical field. As indicated by theory, Ic is insensitive to Hc ($\propto \Delta E/k_BT$).

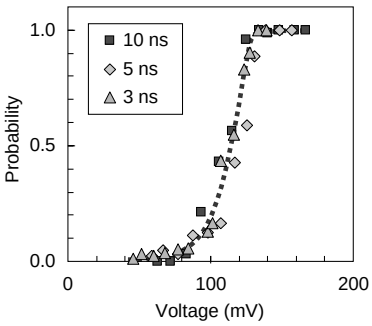


Fig. 6. Dependence of switching probability on pulse duration. DW velocity is estimated to be more than 50 m/s, corresponding to 3-ns switching .

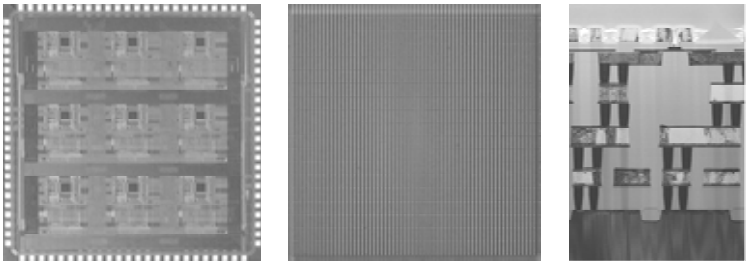

Fig. 7. Photograph of 4k-array and cross-sectional TEM image.

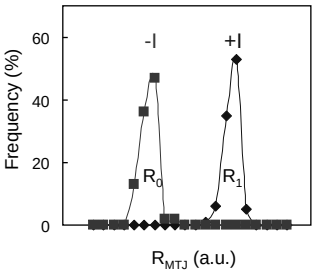


Fig. 8. Histogram of resistance after injecting bidirectional currents. R0 and R1 are clearly separated.

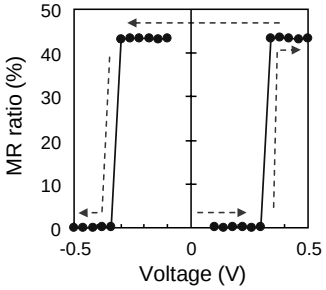


Fig. 9. R-I characteristic for DWM cell.

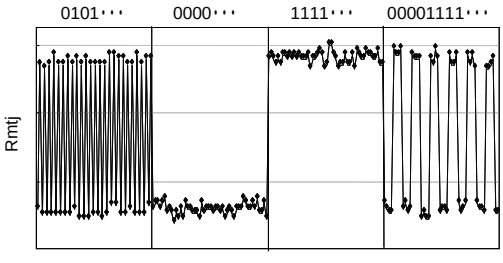


Fig. 10. Repeat test results of the device. Good reproducible switching and overwrite properties were achieved.