Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp310-311

Superiority of ALD TiN with TDMAT Precursor for Metal-Gate MOSFET

T. Hayashida[1], K. Endo[2], Y. X. Liu[2], T. Matsukawa[2], S. Ouchi[2], K. Sakamoto[2], J. Tsukada[2], Y. Ishikawa[2], H. Yamauchi[2], A. Ogura[1], and M. Masahara[1,2],

[1]School of Science and Technology, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa, 214-8571, Japan Tel: +81-44-934-7324, E-Mail: hayashida-meiji@aist.go.jp
[2]National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba Central 2, 1-1-1 Umezono, Tsukuba, Ibaraki, 305-8568, Japan

1. Introduction

Metal gate is the essential technology to reduce the gate depletion and the gate resistance. Recently, an atomic layer deposition (ALD) has been taken much attention due to an excellent thickness controllability and damage free process. It was reported that ALD-TiN gate grown with tetrakis dimethylamino titanium (TDMAT) precursor is very attractive thanks to its excellent thermal stability during the high temperature annealing [1], while the ALD-TiN gate with $TiCl_4$ shows thermal instability [2]. However, there have been no comprehensive studies on device characteristics of MOSFETs using the ALD TiN with TDMAT precursor. In this paper, for the first time, we investigate the superiority of the ALD-TiN-gate MOSFETs using TDMAT precursor comparing with the physical vapor deposited (PVD)-TiN-gate MOSFETs [3].

2. Experiment

As a starting material, p-type (100) bulk Si wafers were used. After the gate oxidation, the TiN metal gate was deposited by the ALD method using the alternate supply of TDMAT and NH_3. The PVD TiN was also used for comparison. The resistivity and the composition of ALD-TiN films were measured. The ALD-TiN-gate MOSFETs were fabricated by using the gate-first fabrication process. After the 5.8-nm-thick gate oxidation, the 11-nm-thick ALD TiN was deposited and then the 100-nm-thick n^+-poly-Si gate was deposited as a capping layer. After the gate patterning, the ion implantation for the source/drain region and the rapid thermal annealing (RTA) at 800^{o}C for 2 s were carried out. Finally, contact holes and aluminum electrodes were formed, and all wafers were sintered in a forming gas ambient at 450^{o}C for 30 min.

3. Characterization of ALD-TiN film with TDMAT

To investigate the optimal temperature range for the ALD-TiN with TDMAT precursor, the growth rate and the resistivity as a function of the substrate temperature (T_{sub}) during the deposition were examined, as shown in Fig. 1. According to the previous report [4], a film thickness of 1 monolayer TiN is 0.36 nm. In this study, 0.36 nm/cycle was achieved at around 200^{o}C. We thus concluded that the T_{sub} must be set below 200^{o}C for maintaining the ALD condition. However, the resistivity was still higher than the films deposited at 300 ^{o}C as also shown in Fig. 1. To explore the characteristics of the ALD-TiN film deposited at 200^{o}C, the composition of the film was evaluated by the XPS analysis, as shown in Fig. 2. The concentration of Ti and N was almost the same and the residual carbon concentration was below 5% in the TiN film. On the other hand, very high oxygen concentration was detected due to the oxidation at the air exposure [1]. Based on this result, it is reasonably concluded that the high resistivity of ALD-TiN film results from the detected high oxygen concentration in the film. To obtain the low resistive TiN films, we tried the 600^{o}C PDA with N_2 or NH_3 ambient after the deposition at 200^{o}C, as shown in Fig. 3. The smallest resistivity was achieved at the PDA with NH_3. This NH_3 annealing may prevent the oxidation by forming the strict Ti-N bond. Thus, we can say that the PDA with NH_3 is the promising way to reduce the resistivity of the ALD-TiN film with TDMAT precursor. This PDA condition was applied to the following ALD-TiN-gate MOS capacitor and MOSFET device fabrication process.

4. TiN-gate MOS capacitors

Figure 4 shows the RTA temperatures (T_R) dependence of the C-V characteristics of the fabricated TiN-gate MOS capacitors measured at the frequency of 1 MHz. For comparison, C-V characteristics of the PVD-TiN-gate MOS capacitors are also shown. The work function (WF) of the PVD TiN (w/o RTA) was 4.87 eV [5]. On the other hand, the WF of the ALD-TiN gate (w/o RTA) was smaller than that of PVD TiN and was estimated at 4.2 eV. This lower WF for ALD TiN is probably due to the Ti rich concentration just at the metal-insulator interface [1]. It should be noted that, in the case of the ALD TiN, no degradation in C-V characteristics occurs after the RTA, while the significant degradation occurs in the case of PVD TiN. This indicates that the thermal stability of the ALD TiN is higher than that of the PVD TiN. As shown in Fig. 5, T_R dependence on the interface trap density (D_{it}) was investigated using the low-frequency C-V method [6]. The frequency dependences of the C-V curves were clearly observed with the PVD-TiN-gate MOS capacitors, which means the higher D_{it}. Figure 6 compares the D_{it} peaks of the ALD- and the PVD-TiN -gate MOS capacitors as a function of T_R. The D_{it} for the ALD TiN was much lower than that of PVD TiN regardless of T_R. Note that the D_{it} for the ALD TiN was less also w/o RTA. This clearly shows that the ALD-TiN process hardly introduces the physical damage during the deposition.

5. Characteristics of TiN-gate MOSFETs

Figure 7 shows the I_d-V_g and G_m-V_g characteristics for the fabricated ALD- and PVD-TiN-gate MOSFETs. It is noteworthy that both s-slope and G_m for the ALD-TiN -gate MOSFET were superior to those for PVD-TiN-gate

MOSFET. This is because the ALD TiN shows lower D_{it} than the PVD case, as shown in Fig. 6. Figure 8 shows the electron mobility of the ALD- and PVD-TiN-gate MOSFETs. In the case of ALD TiN, 30% higher mobility can be achieved compared with the PVD TiN.

6. Summary

We have investigated the superiority of the ALD-TiN gate using the TDMAT precursor comparing with the PVD TiN. It was found that the NH_3 PDA at 600°C is very promising to lowering the resistivity of ALD-TiN films. The WF of the ALD-TiN gate (w/o RTA) was roughly estimated at 4.2 eV. D_{it} for ALD TiN was much lower than that for PVD TiN regardless of the RTA conditions. Thanks to lower D_{it}, superior s-slope and mobility were obtained for the ALD-TiN-gate MOSFETs as compared with the PVD-TiN-gate MOSFET. Thus we can conclude that ALD TiN using TDMAT precursor is the proper gate material for the gate first fabrication process.

Acknowledgement

This work was supported in part by the METI's Innovation Research Project on Nanoelectronics Materials and Structures. XPS measurements were conducted at the AIST Nano-Processing Facility, supported by "Nanotechnology Network Japan" of MEXT.

References

[1] F. Fillot et al., Microelectric Engineering 82(2005) p248
[2] J. Weslinder et al., IEEE Electron Dev. Lett. Vol. 24, no. 9, (2003), p550
[3] T.Hayashida et al., Jpn. J. Appl. Phys, vol 48, no. 5, (2009) 05DC01
[4] J.-S.Min et al., Jpn. J. Appl. Phys, vol.37 (1998) pp.4999
[5] Y.X.Liu et al., Jpn. J. Appl. Phys, vol 47, no. 4, (2008) pp.2433
[6] D.K.Schroder : Semiconductor Material and Device Characterization (Wiley, New York, 1998) 2nd ed. P371

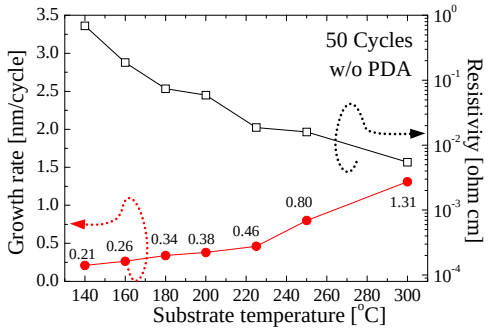

Fig. 1. T_{sub} dependence of the growth rate and the resistivity for the as deposited ALD-TiN films.

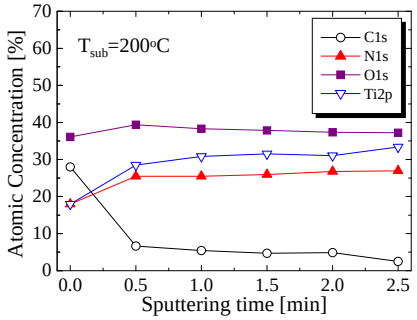

Fig. 2. The atomic concentration of the as deposited ALD-TiN film deposited at 200°C as a function of sputtering time by the XPS analysis.

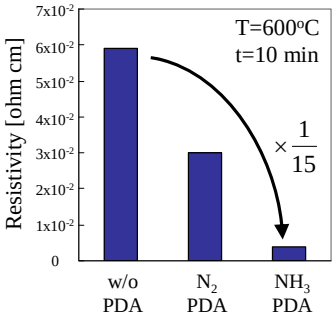

Fig. 3. The resistivity of the ALD-TiN gate with various PDA conditions.

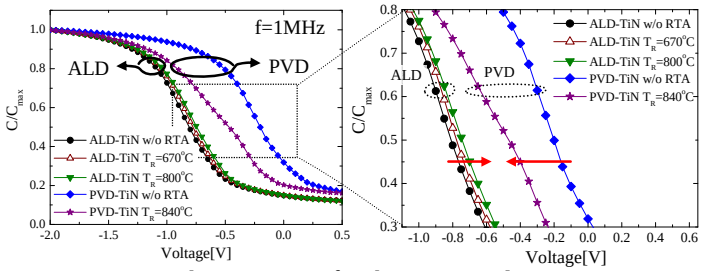

Fig. 4. C-V characteristics for the ALD- and PVD-TiN-gate MOS capacitors with various T_R measured at frequency of 1 MHz.

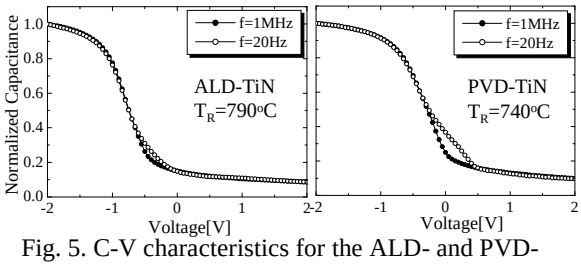

Fig. 5. C-V characteristics for the ALD- and PVD-TiN-gate MOS capacitors measured at frequency of 1 MHz and 20 Hz.

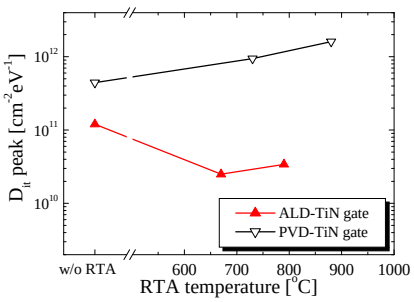

Fig. 6. T_R dependence of D_{it} peak of the fabricated ALD- and PVD-TiN-gate MOS capacitors.

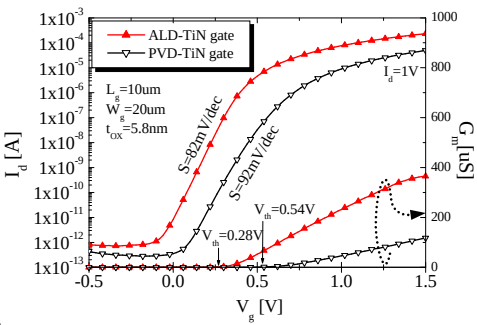

Fig. 7. I_d-V_g and G_m-V_g characteristics and trans-conductance of the ALD- and PVD-TiN-gate MOSFETs.

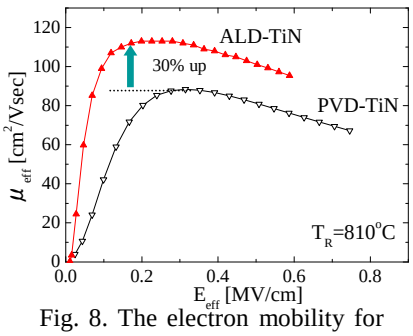

Fig. 8. The electron mobility for the ALD- and PVD-TiN-gate MOSFETs.