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Nanoscale Characterization of HfO_2/SiO_x Gate Stack Degradation by Scanning Tunneling Microscopy

K. S. Yew[1+], Y. C. Ong[1], D. S. Ang[1], K. L. Pey[1], G. Bersuker,[2] P. S. Lysaght[2], and D. Heh[2]

[1]Nanyang Technological University, School of Electrical and Electronic Engineering, Singapore 639798 (E-Mail[+]: E080086@ntu.edu.sg)

[2]SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741-6499, USA

1. Introduction

Conventional TDDB test has provided valuable insight into the mechanism of SiO_2 gate dielectric breakdown (BD) but the same approach applied to the high-κ gate stack gives conflicting outcomes: (1) Some authors[1] inferred that BD was controlled by the ultrathin SiO_x interfacial layer (IL), on basis that the BD characteristics were similar to those of a single ultrathin SiO_2; (2) Others deduced that BD was controlled by the high-κ as abrupt BD typical of that in a thick SiO_2 was observed[2]. A major shortcoming of conventional TDDB test is its lack of ability to resolve microscopic changes which ultimately governs BD. This is particularly crucial for the high-κ gate stack in which a high degree of inhomogeneity preexists inherently. In this work, degradation of the HfO_2/SiO_x gate stack was studied via Scanning Tunneling Microscopy (STM) at the nanoscale level. We observe substantial increase of tunneling leakage through the IL at locations where leakage paths preexist or are induced by electrical stress in the high-κ. This suggests that IL controlled BD is a consequence of "pre-breakdown" in the high-κ.

2. Experimental

Gate stack comprising 5nm HfO_2 on top of a 1nm SiO_x was formed by atomic layer deposition on a p-Si substrate. Post-deposition annealing was carried out at 700ºC. STM was performed in ultrahigh vacuum at 25ºC. The bias voltage V_s was applied to the substrate. The gate stack was scanned at a bias set-point of V_s = +5V and I = 90pA over a 500nm × 500nm area. Local variations of the tip height at a constant tunneling current were recorded to form the constant current image (CCI). Constant Current Tunneling Spectroscopy (CITS) was performed to examine the local electrical conductivity of the gate stack. The feedback circuit was temporarily disabled after the preset tunneling current was achieved, and V_s was swept from +5V to −5V, at every pixel of the scanned area. The corresponding tunneling spectra were recorded to form the CITS current map.

3. Results and Discussion

Since the tunneling current is most sensitive to the barrier height at the emitting electrode[3], CCI obtained at positive V_s is primarily a manifestation of the topography and electronic property of the high-κ. Electronic property of the IL may be examined via a CITS map at negative V_s in conjunction with local I-V curves. Fig. 1 shows a series of CCIs of the HfO_2/SiO_x gate stack for 9 consecutive scans. Bright spots correspond to locations where retraction of the metal tip was recorded. The tip retracts when it moves over a high leakage path (as a greater vacuum spacing is needed to maintain a constant current) or a physical protrusion on the surface (i.e. surface roughness).

A. IL Degradation at Preexisting High-κ Leakage Paths

Analysis done on bright spot A shows that it arises out of a physical "bump" on the high-κ surface. This is inferred based on the "inverted contrast" of the CCI and CITS map shown in Fig. 2(a) and (b), respectively [i.e. what appears to be bright in Fig. 2(a) appears dark in Fig. 2(b)]. Close examination of the CITS map [Fig. 2(b)] reveals, within spot A, localized dark regions (denoted by dotted lines) surrounded by brighter borders. This suggests that spot A is made up of a cluster of grains; the dark regions correspond to the grains and the brighter circumference (dash-dot lines) to the grain boundaries. The height and current profiles along line 1,2 exhibit opposite trend, further confirming this inference. The tunneling spectra at the grain and grain boundary are extracted from the 1st and 9th scan. As depicted in Fig. 3, tunneling current in the negative V_s regime (henceforth denoted as "negative-I_t") is much higher at the grain boundary in the very 1st scan. The current remains unchanged at the grain while it is increased by ~33% at the grain boundary after repeated scans. This shows that the IL is subjected to a higher electrical stress at locations where a leakage path preexists in the high-κ.

B. IL Degradation without Preexisting High-κ Leakage Path

In contrast to bright spot A, bright spots C, D and E appear gradually from the 6th can [Fig. 1(f)] onwards. This means that C, D, and E are electrically induced and is not topography related. As depicted in Fig. 4, the negative-I_t at spot C remains unchanged at the 5th and 6th scan, implying no degradation of the IL. The subtle appearance of C at the 6th scan [Fig. 1(f)] therefore implies the onset of HfO_2 degradation. At the 7th scan, the negative-I_t increases substantially, corresponding to more substantial degradation of HfO_2 (as inferred from the increased brightness and size of C). [Fig. 1(g)]. The same observations apply to D and E. Likewise, the negative-I_t at bright spot F in Fig. 5 is remains relatively unchanged (despite repeated scans) in the absence of a leakage path in the high-κ. However, the tunneling current increases significantly at the 8th scan; note that F appears [Fig. 1(h)] at the locations where there were no bright spots previously [Fig. 1(g)]. This observation signifies that the electronic trap generation occurs in the high-κ initially. When a leakage path is formed in the high-κ, the IL begins to degrade rapidly. The appearance and the gradual growth of the bright spots in the topography map in Fig. 1 signify the formation of the leakage paths in the high-κ layer as a result of the electrical resistivity drop at those particular locations. The presence of leakage paths in turn causes a substantial reduction in the voltage drop across the high-κ layer at these locations and hence, the IL directly underneath the leakage paths are forced to sustain a higher electric field under applied voltage stress. A larger electric field increases the tunneling current through the IL and accelerates its degradation, as seen by the substantial increase in the negative-I_t when a bright spot is observed in the corresponding CCI.

4. Summary

Nanoscale characterization of the HfO_2/SiO_x gate stack using STM is presented. Results show that degradation and BD of the IL depends ultimately on the state of the much thicker high-κ. Wherever a leakage path (whether preexisting or stress induced) is present in the high-κ, significant degradation of the underlying IL (as revealed by the tunneling spectra under substrate injection bias) is observed, triggering BD of the entire gate stack. We show directly that the IL beneath a grain boundary (leakage path) in the high-κ layer is more susceptible to degradation under electrical stress.

References

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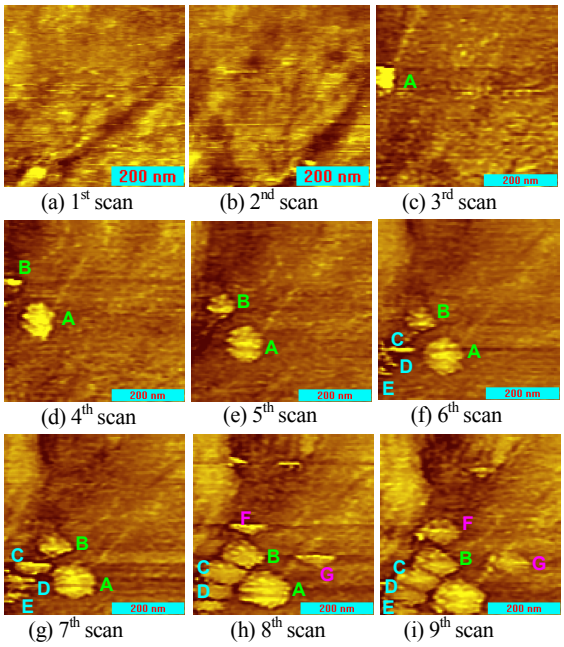
[2] Sato *et al.*, JJAP (47), 3326, 2008
[3] Ong *et al.*, Appl. Phys. Lett. (92), 022904, 2008

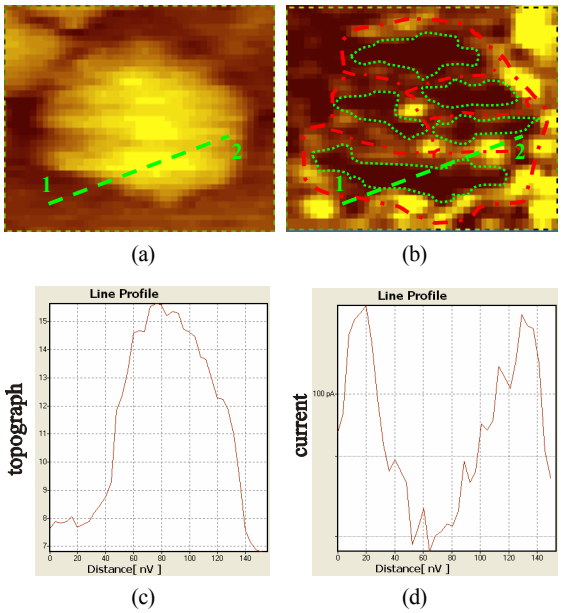


(a) 1st scan (b) 2nd scan (c) 3rd scan

(d) 4th scan (e) 5th scan (f) 6th scan

(g) 7th scan (h) 8th scan (i) 9th scan

Fig. 1 Constant current STM image (CCI) of the HfO_2/SiO_x gate stack for 9 consecutive scans; bias set point: V_s = +5V, I = 90pA. The colour contrast in the topography map is attributed to local variation in the gate stack thickness and/or conductance over the scanned area of 500nm × 500nm. The bright spots in the image are observed to have shifted slightly for every subsequent scan due to thermal drift. Two distinct observations: (i) Bright spots A and B exist at the early stage of the scans, at the 3rd and 4th scan, respectively. (ii) Bright spots C, D, E, F and G appear gradually at area of relatively uniform contrast at later scans; at the 6th scan (8th scan) for C, D and E (F and G).



(a) (b)

(c) (d)

Fig. 2 (a) Zoom-in view of bright spot A in Fig. 1 (h); bias set point: V_s = +5V, I = 90pA. (b) Corresponding CITS map at V_s = –5V; green dotted line and red dash-dot line denote the grains and grain boundaries, respectively. (c) and (d) depict the height and current profiles, respectively along line 1,2 as indicated in (a) and (b).

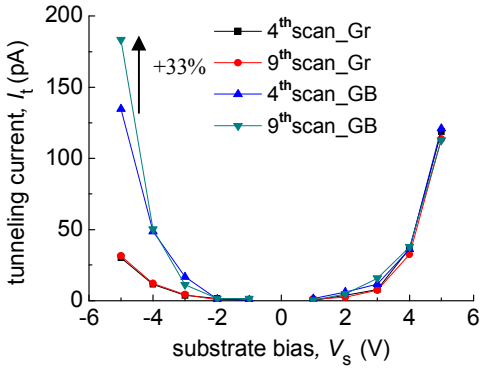


Fig. 3 Tunneling spectra of a grain (4thscan_Gr and 9thscan_Gr) and a grain boundary (4thscan_GB and 9thscan_GB) within bright spot A, extracted from the CITS current map corresponding to the CCI in Fig.1 for the 4th and the 9th scans only. In the negative V_s regime, the tunnelling current at the grain boundary is increased whereas that at the grain shows no increase after 9th scan. Tunneling spectra in the positive V_s regime all coincide because they are normalized to the same bias set-point (+5V, 90pA).

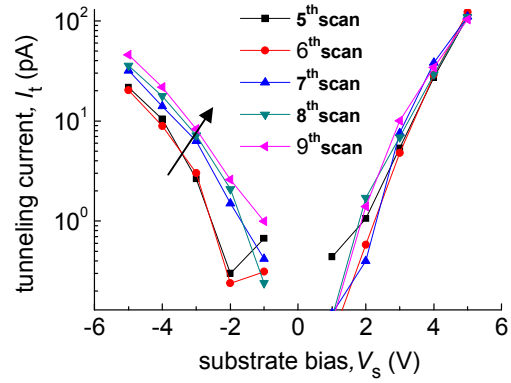


Fig. 4 Tunneling spectra of bright spot C, extracted from the CITS current map corresponding to the CCI in Fig.1 between 5th scan and 9th scan. Bright spot C appears slowly at the 6th scan [Fig.1 (f)] and it becomes more evident at the 7th scan [Fig.1 (g)]. In the negative V_s regime, the tunnelling current does not increase initially (5th scan and 6th scan), but it increases significantly at the 7th scan. Both 8th and 9th scans show slight increase.

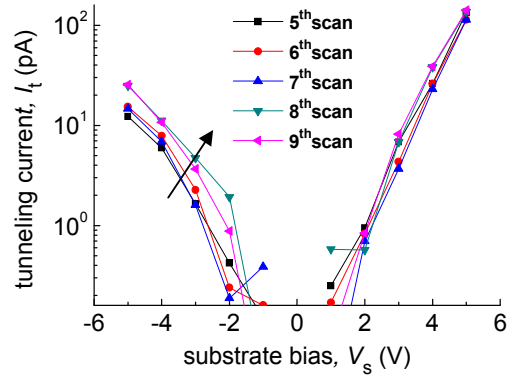


Fig. 5 Tunneling spectra of the bright spot F extracted from the CITS current map corresponding to the CCI in Fig.1 between 5th scan and 9th scan. Bright spot F begins to appear at the 8th scan [Fig. 1(h)]. In the negative V_s regime, the tunnelling current does not increase much initially (5th, 6th and 7th scans), but it increases significantly at the 8th scan.