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Voltage Coefficient of Capacitance Modulation for Sm_2O_3/SiO_2 MIM Capacitors

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1. Introduction

Metal-insulator-metal (MIM) capacitor is one of the essential passive components in the radio-frequency and analog IC applications. High capacitance density and low voltage coefficient of capacitance (VCC) are needed [1]. High-κ dielectrics are therefore investigated. However, many high-κ dielectrics show large quadratic VCC, which is unacceptable for precision analog circuit applications [2, 3]. Recently, stacking of HfO_2 layer with thin SiO_2 layer (having negative quadratic VCC) has been demonstrated to effectively modulate the VCC [4]. However, further improvement is limited by the large positive quadratic VCC of HfO_2. Sm_2O_3 is found to show a smaller quadratic VCC as compared to HfO_2. Moreover, the plasma treatment can reduce the VCC for Sm_2O_3 MIM further. In this work, we report the use Sm_2O_3 instead of HfO_2 to further modulate the capacitance density and VCC through stacking with SiO_2. Sm_2O_3/SiO_2 MIM capacitors with superior capacitance densities and comparable VCC with respect to the HfO_2/SiO_2 stack were obtained.

2. Experiment

MIM capacitors were fabricated on Si wafers covered with 500 nm thick SiO_2. A 200 nm thick sputtered TaN layer was first deposited on SiO_2 as bottom electrode. For Sm_2O_3 MIM capacitors, Sm_2O_3 was deposited on bottom TaN electrode by sputtering. For Sm_2O_3/SiO_2 MIM capacitors, thin SiO_2 with various thicknesses (3, 3.5, 4, 5, and 7 nm) were deposited on TaN by PECVD at 350 °C, and Sm_2O_3 (6.5, 7.5, 8.5 and 10 nm) was then deposited on PECVD SiO_2. After dielectric deposition, optional Plasma Treatment in N_2 ambient (PTN) was carried out. Post deposition annealing at 400 °C for 120 s in N_2 ambient was then performed. Finally, a 150 nm thick TaN layer was sputtered and patterned to form the top electrode.

3. Results and discussion

(a) VCC Improvement of Sm_2O_3 MIM Capacitors by PTN

Fig. 1 compares the quadratic VCC of HfO_2 and Sm_2O_3 MIM (with or without PTN on dielectrics). MIM capacitors with Sm_2O_3 dielectric, especially those with PTN, are found to show smaller positive quadratic VCC as compared to those with HfO_2 layer. Moreover, for Sm_2O_3 MIM capacitors, we have inserted the PTN process after formation of bottom electrode, after dielectric layer formation, or at both steps. The normalized *C-V* curves in Fig. 2(a) compares the effects of different PTN on the VCC of MIM capacitors with Sm_2O_3 dielectric. Fig. 2 (b) summarizes both the quadratic and linear VCC of Sm_2O_3 MIM capacitors with different PTN conditions. Performing PTN directly after dielectric formation achieves the smallest quadratic and the smallest linear VCC, which are important parameters for precision analog circuit applications. This indicates that PTN on dielectric can improve the VCC of Sm_2O_3 MIM capacitor.

(b) Effective VCC Modulation of Sm_2O_3/SiO_2 MIM Capacitors

The smaller quadratic VCC of MIM capacitors with Sm_2O_3 dielectric as compared to that with HfO_2 dielectric implies that Sm_2O_3 is more suitable than HfO_2 for exploitation of the "cancelling effect" using SiO_2 [4]. A simulation is first carried out to determine the relationship between the quadratic VCC and the stacked dielectric thicknesses (Fig. 3). For a thinner Sm_2O_3 thickness, a more precise thickness control for SiO_2 is needed.

Fig. 4(a) depicts the TEM image of a Sm_2O_3/SiO_2 stack with their thicknesses at 7.5 nm/3.5 nm. Note that all the MIM capacitors with Sm_2O_3/SiO_2 dielectric stack presented here have the PTN performed after dielectric formation. Fig. 4(b) shows the normalized *C-V* curves of MIM capacitors with Sm_2O_3 thickness fixed at 7.5 nm and SiO_2 thicknesses varying from 3 to 7 nm. The dark lines are *C-V* curves of Sm_2O_3 and SiO_2 MIM capacitors with comparable capacitance densities. Increasing the SiO_2 thickness can effectively modulate the quadratic VCC from positive to negative values. Fig. 5(a) summarizes the quadratic VCC versus capacitance density with varying SiO_2 thicknesses from 3 to 7 nm for Sm_2O_3 thicknesses at 6, 7.5, 8.5, and 10 nm respectively. For each Sm_2O_3 thickness, the quadratic VCC can be adjusted to hit the target range of quadratic VCC within ±100 ppm/V^2 by controlling the thickness of SiO_2 in the Sm_2O_3/SiO_2 stack [Fig. 5(b)]. This is similar to the aforementioned simulation result shown in Fig. 3. High capacitance densities of above 7.3 fF/μm^2 and quadratic VCC within ±100 ppm/V^2 are successfully demonstrated with Sm_2O_3/SiO_2 thickness of 7.5 nm/4 nm, 6.5 nm/4 nm and 6.5 nm/3.5 nm, respectively. Also from the change of the quadratic VCC with capacitance density, it is possible to achieve capacitance density of over 8 fF/μm^2 and quadratic VCC of near zero by optimizing the thickness ratio of SiO_2 (or Sm_2O_3) to whole dielectric stack. The linear VCC of these Sm_2O_3/SiO_2 MIM capacitors are summarized in Fig. 6. It is shown that the linear VCC is also modulated by tuning the thickness of SiO_2.

Fig. 7 summarizes the leakage (at +3.3 V) versus capacitance density of these Sm_2O_3/SiO_2 MIM capacitors. Leakages can be maintained at around 1.0×10^{-7} A/cm^2 at +3.3 V (room temperature) or even less. Fig. 8(a) shows the influence of the temperature on the *J-V* curves for the laminate capacitors with Sm_2O_3 at 8.5 nm and SiO_2 at 3.5 nm. The asymmetric *J-V* curves are due to the asymmetric dielectric stacks and different dielectric-electrode band offsets [5]. The different *J-V* behaviors at low and high bias region (> 2.5 V) reflect the different current transport mechanisms. The conduction process at high bias is likely to be dominated by Poole-Frenkel emission [Fig. 8(b)].

4. Conclusions

We demonstrated the VCC improvement for Sm_2O_3 MIM capacitors by using PTN on dielectrics and the effective VCC modulation for Sm_2O_3/SiO_2 MIM capacitors by using Sm_2O_3/SiO_2 stack. High capacitance densities (above 7.3 fF/cm^2), low quadratic VCCs (within ±100 ppm/V^2), and low leakages at +3.3 V (1.0×10^{-7} A/cm^2) are obtained by using the "cancelling effect" through stack combination of SiO_2 and Sm_2O_3. The Sm_2O_3/SiO_2 MIM capacitors can achieve higher capacitance density and near zero quadratic VCC through further optimization of the Sm_2O_3/SiO_2 thickness ratio. High capacitance density and low quadratic VCC reported here satisfy the requirements of MIM capacitors in precision analog circuit applications till year 2013 according to ITRS 2007.

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References.

[1] http://www.itrs.net/reports.html. [2] H. Hu *et al.*, *IEEE EDL*, v. 23, pp. 514 (2002). [3] S. B. Chen *et al.*, *IEEE EDL*, v. 23, pp. 185 (2002). [4] S. J. Kim *et al.*, *Symp. VLSI Tech.*, pp. 218 (2004). [5] R. Degraeve *et al.*, *Proc. IRPS*, pp. 23. (2003).

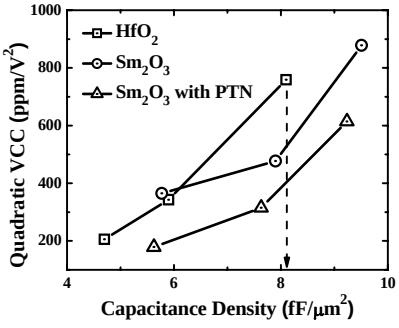


Fig. 1. Quadratic VCC (α value) versus capacitance density of HfO_2 and Sm_2O_3 (with or without PTN). Sm_2O_3 MIM with PTN on Sm_2O_3 dielectrics can obtain much lower quadratic VCC.

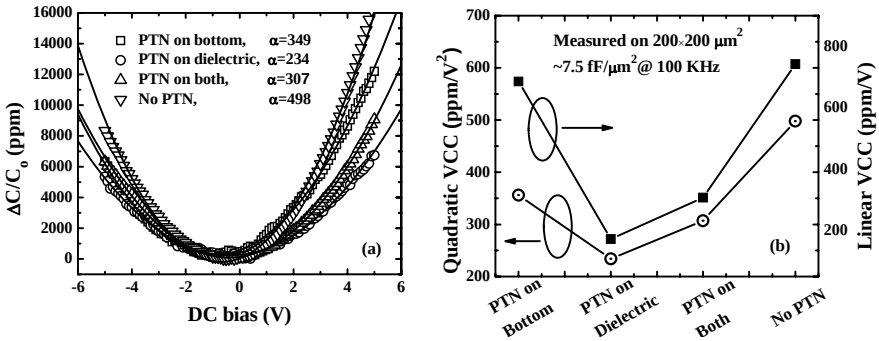


Fig. 2(a). Normalized *C-V* curves of Sm_2O_3 MIM capacitors with or without optimized PTN on bottom electrode, dielectrics, and both bottom electrode and dielectrics. **(b)** Summary of the quadratic and linear VCC of Sm_2O_3 MIM capacitors after different PTN. The best VCCs are obtained by using PTN directly on dielectrics.

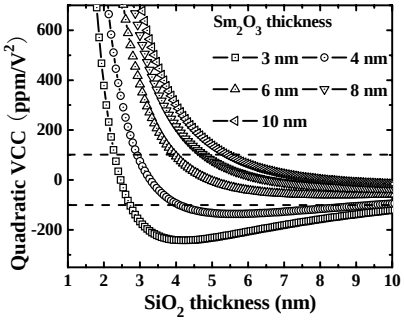
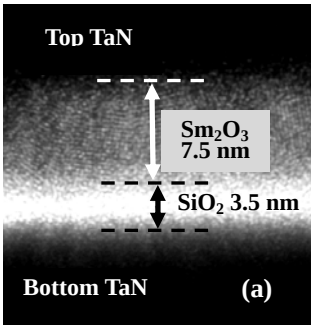


Fig. 3. Simulated result of quadratic VCC versus SiO_2 thickness with varying Sm_2O_3 thicknesses. The quadratic VCC is sensitive to the thicknesses of both SiO_2 and Sm_2O_3.



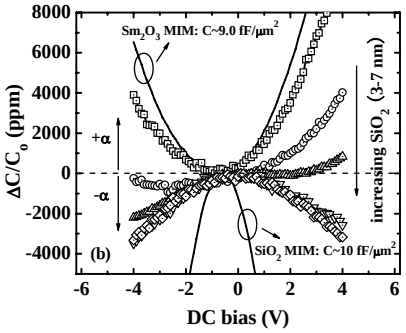


Fig. 4(a). TEM image of stacked Sm_2O_3/SiO_2 MIM capacitor. **(b)** Normalized *C-V* curves of Sm_2O_3/SiO_2 MIM capacitors with SiO_2 thickness varying from 3, 3.5, 4, 5, to 7 nm, and Sm_2O_3 thicknesses being fixed at 7.5 nm. Sm_2O_3 and SiO_2 MIM with comparable capacitance densities are also included. The effective quadratic VCC (α value) is modulated from positive to negative values by increasing SiO_2 thickness.

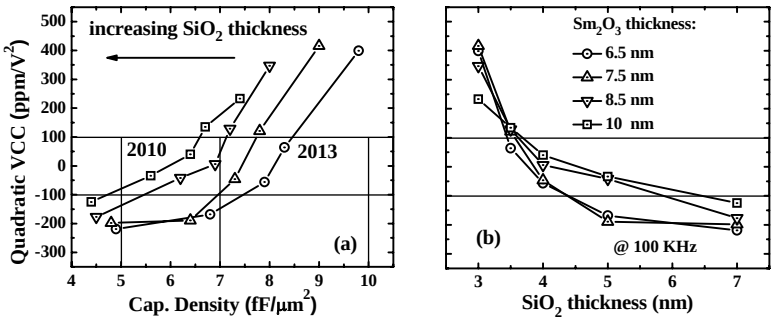


Fig. 5(a). Quadratic VCC versus capacitance density and **(b)** Quadratic VCC versus SiO_2 thickness (3 to 7 nm) for Sm_2O_3 thicknesses being varied (6.5, 7.5, 8.5, and 10 nm). Near zero α value can be obtained by optimizing the thickness ratio of SiO_2 (or Sm_2O_3) to Sm_2O_3/SiO_2 stack. The capacitance density and quadratic VCC can be modulated to meet the requirements of MIM capacitors till 2013 [1].

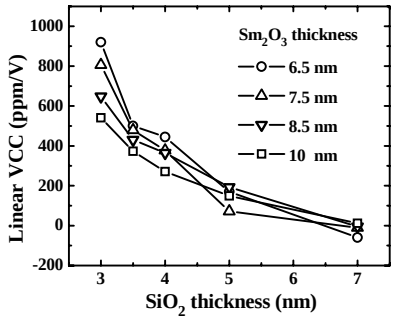


Fig. 6. Linear VCC versus SiO_2 thickness with varying the thickness of SiO_2 and Sm_2O_3. The linear VCC can be modulated to near zero by increasing the thickness of SiO_2.

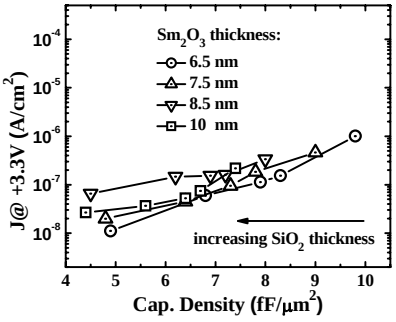


Fig. 7. Summary of the leakage current densities of Sm_2O_3/SiO_2 MIM capacitors with various combinations of Sm_2O_3 (6.5, 7.5, 8.5, and 10 nm) and SiO_2 (3 nm to 7 nm) thicknesses.

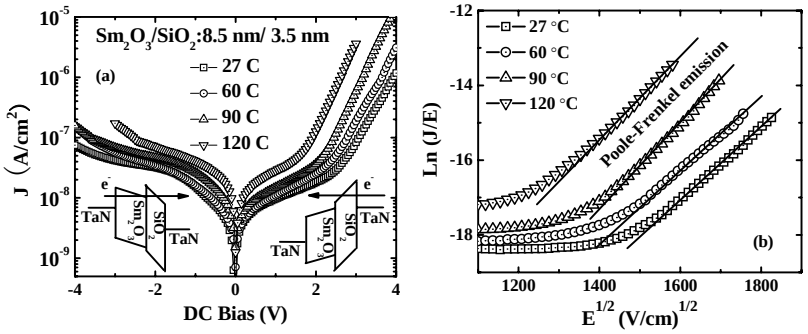


Fig. 8(a). *J-V* curves of Sm_2O_3/SiO_2 capacitors with an 8.5 nm thick Sm_2O_3 and a 3.5 nm thick SiO_2 measured from 27 to 120 °C. **(b)** Ln(*J*/*E*) versus $E^{1/2}$ at different temperatures measured at high positive bias. *P-F* emission likely dominates in this region from the room temperature to 120 °C.