Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp294-295

Advanced high-k materials and electrical analysis for memories: the role of SiO_2-high-k dielectric intermixing

L. Morassi[1], L. Larcher[1], L. Pantisano[2], A. Padovani[1], R. Degreave[2], M. B. Zahid[2], B. J. O'Sullivan[2]

[1] Università di Modena e Reggio Emilia and IU.NET, Via Amendola 2, 42100 Reggio Emilia, Italy
Phone: +39-0522-522638 E-mail: andrea.padovani@unimore.it - [2]IMEC Kapeldreef 75

Different high-k materials have been recently investigated for IPD (Al_2O_3 or SiO_2/Al_2O_3 [1]) and tunnel layers (SiO_2 or $SiO_2/Hf_2O/SiO_2$ [2]). Trap energies and densities are crucial to control reliability specs like retention and programming and erasing times. The fundamental question is then *how to control and characterize these dielectrics*? One of the roadblocks is how to control the chemistry at submonolayer level, especially at interfaces where intermixing is likely to occur and where the electrical characteristics are more vulnerable.

This paper presents an original approach for material studies for memory devices where the degree of intermixing between the high-k and interfacial SiO2 is explicitly quantified experimentally. Using calibrated leakage simulation the importance of intermixing is verified independently together with the conduction mechanism. The implication for NVM reliability are profound and will be discussed toward retention mechanisms and used to optimize retention margins for NVM memories.

The slant etch experiment. Conventional MOSFET with high-k/MG were considered. Starting surface was either thermal SiO_2 (1-3nm) or slanted SiO_2. In the latter a thick thermal SiO_2 is chemically etched such as to achieve a linear t_{SiO2} variation (see Fig. 1) across the wafer (from 1 to ~4nm). Note that the chemical HF-based etch does not affect the SiO_2 quality as shown in fig. 2. Either ALD 10-nm Al_2O_3 with PDA 1000C in N_2 or HfSiO film of 2-nm thickness (60%Hf 40%Si) deposited by ALD with PDA 900C in N_2 were considered as high-k. The gate electrode was 10-nm TaN, deposited by sputtering, followed by a 1030C spike anneal for dopant activation [3]. The thick SiO_2 portion mimics the TANOS gate stack.

Bulk and intermixing layer characterization. Together with a slant-etch SiO_2, different techniques were considered to probe defects in the HK stack and in the intermixing. Fig.3 shows the *near interface* defects extracted from slanted SiO_2/Al_2O_3 stacks using VT2CP [4]. As in [4], for the 1nm EOT IL both the IL and the Al_2O_3 quality is quantified *simultaneously*, while this is not the case for Thicker IL, (i.e., only the IL-defects are scanned). Unfortunately, only a qualitative understanding is possible.

For a more quantitative understanding, we used TSCIS to scan defects in the bulk material [5]. For a given high-k, varying the IL thickness *on the same wafer* allows performing the defect spectroscopy of both IL (i.e., thick IL) and bulk HK defects (i.e., thin IL). Defect density and energy spectroscopy results are shown for two extreme IL cases in fig.4. Note the defects ~ $10^{20}/cm^3eV^{-1}$ in both cases. When the 3nm IL is considered, defects are much closer to the Si interface than expected from the stack thicknesses, suggesting a severe intermixing between SiO_2 and Al_2O_3. Note that defects in 3nm IL have similar densities compared to the 1nm IL in the Al_2O_3 bulk. Bulk Al_2O_3 defects are rather deep, being roughly 0.6-0.8eV higher than the Si conduction band.

The intermixing between SiO2 and Al2O3 is severe. In order to gain more quantitative insights, we derived defect densities and energies by using leakage current simulations performed with the statistical physic-based model presented in [6]. This model assumes the multi-phonon trap assisted tunneling as the conduction mechanism. Moreover, it includes quantization effects and random defect generation inside SiO_2, intermixing and HK layers, see Fig. 5. As shown in Fig. 6, simulations reproduce very accurately leakage currents measured on slant etch samples for both gate and substrate injection by using a unique set of physical parameters for defects, see Table I. Noticeably, simulations allow evaluating the thickness of the intermixing layer, t_{IML}=1.8nm, which is consistent with the formation of AlSiOx reported during deposition [7]

The results on Al2O3 agree with earlier reports from Afanas'ev et al, where the AlSiOx formation where measured by internal photoemission. Defect densities and energies agree also very well with those estimated using TSCIS technique. Interestingly, for gate injection the carrier transport at low field is limited by the metal gate/high-k barrier while at high field the hole contribution becomes very important.

An important benchmark for this approach is the HfSiO case. Note that HfSiO is more thermally stable than Al_2O_3. Following the same methodology, we characterized also slanted SiO_2/HfSiO samples. Importantly the defect density near the interface is much lower. Again, VT2CP data show the increase of interfacial/bulk defects as the SiO_2 gets thinner (not shown here for brevity). For a more quantitative picture, we used leakage current simulations to extract defect parameters (see Table II) and the thickness of HfSiO-SiO_2 intermixing region, sketched in Fig. 7. As shown in Fig. 8, the agreement between measurements and simulations (obtained with a unique set of parameters) is excellent independently of the SiO_2 thickness. Further, the high defect density of the intermixing is consistent with the expected higher concentration of O vacancies in the HfSiO-SiO_2 transition layer, which depends on the thermal budget and oxygen availability in the system. Interestingly, the energy level of defects in the intermixing is similar to the HK ones for both Al_2O_3 and HfSiO cases, suggesting the same physical origin.

Reliability implications for memories. Defective intermixing layer can play a significant role in NVM retention. The improvement of the tradeoff between program/erase performances and data retention requires to optimize IPD and tunnel stacks. In this scenario, a direct analysis of the defective interlayer impact is not trivial due to the long times involved in data retention characterization. Thus, we used statistical simulations of the leakage current (J_{LEAK}) through HK stacks to assess the *impact of intermixing layer* on their retention [6]. Results are shown in Fig. 9 for Al_2O_3 stack (HfSiO results are not shown here for brevity). As expected, a larger IL benefits the data retention thanks to the reduction in the average loss current. Noticeably, the impact of intermixing layer in retention conditions (i.e. V_G~1.5-2V) rises as the IL gets thinner, increasing J_{LEAK} far beyond the limit ~$2\cdot10^{-16}$ A/cm^2 [8] required to satisfy retention requirements. Thus, the accurate intermixing layer characterization is very important to investigate the feasibility HK stacks in TANOS memories.

Conclusions We used a new methodology to characterize intermixing layer properties in Al_2O3 and HfSiO stacks NVM applications. Using independent experimental techniques and simulations coupled with a simple fabrication technique, we consistently extracted spatial and energy features of both IL and bulk HK defects. Statistical leakage current simulations were used to evaluate the impact of the intermixing layer on NVM data retention.

References [1] Breuil et al. NVSMW/ICMDT 2008; [2] Verma *et al.* IMW 2009; [3] O'Sullivan *et al.* TED Vol.54(7) 2007; [4] Zahid *et al.* IRPS 2009; [5] Degraeve *et al.* IEDM 2008; [6] Padovani *et al.* IRPS 2008; [7] Afanas'ev *et al.* App. Phys. Rev. 2007; [8] Verma *et al.* DRC 2008.

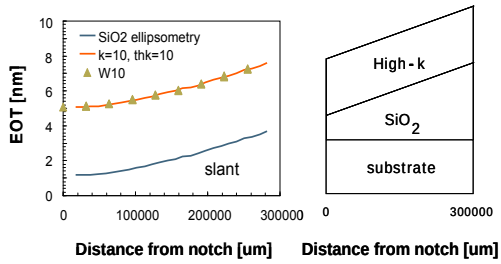

Fig. 1. EOT derived from CV measurements along the slant-etch wafer with SiO_2/Al_2O_3 stack. The schematic cross section of the wafer is shown on the right.

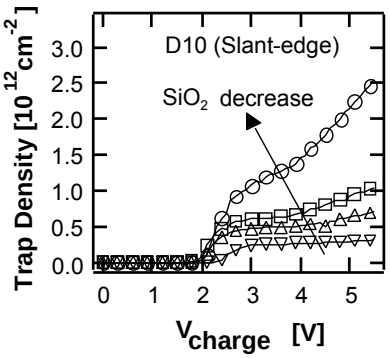

Fig. 3. Trap density vs. charging voltage derived using VT^2CP with $t_{discharge}=t_{charge}$= 1ms for different slanted SiO_2 thickness (from 1nm to 3nm SiO_2). More traps are sensed for thinner SiO_2. Note that CP does not permit to scan traps deeper than ~1.5nm from Si/SiO_2 interface[4].

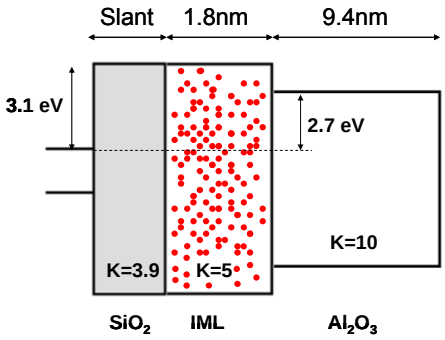

Fig. 5. Schematic band diagram of the simulated SiO_2/Al_2O_3 stack including intermixing layer. IML thickness was kept constant for all the slanted stacks.

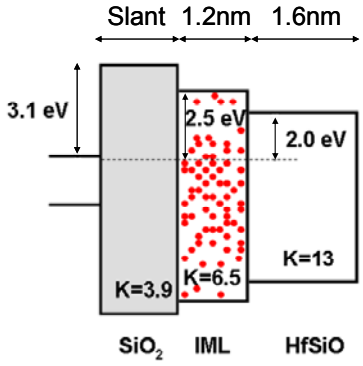

Fig. 7. Schematic band diagram of the simulated SiO_2/HfSiO stack including intermixing layer. IML thickness was kept constant for all the slanted stacks.

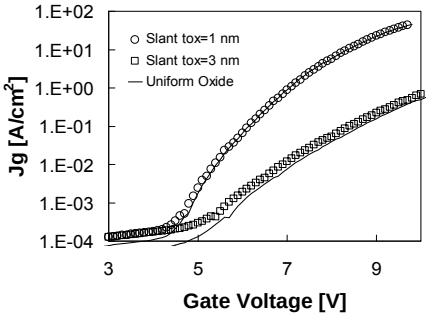

Fig. 2. Leakage currents measured on pure SiO_2 slant-etch wafer (symbols) and thermally grown oxides (lines). The very good agreement proves that the slant-etch technique does not degrade the oxide quality.

Table II : trap parameters for HfSiO stack

Material	Trap Density (N_T)	Energy Level (E_T)
SiO_2	$2\cdot10^{17}$ cm^{-3}	1.6-2.0eV
IML	$1.2\cdot10^{19}$ cm^{-3}	1.0-2.1eV
HfSiO	$4\cdot10^{19}$ cm^{-3}	1.1-1.6eV

Table I : trap parameters for Al_2O_3 stack

Material	Trap Density (N_T)	Energy Level (E_T)
SiO_2	$5\cdot10^{17}$ cm^{-3}	1.5-2.0eV
IML	$5\cdot10^{19}$ cm^{-3}	1.6-2.1eV
Al_2O_3	$9\cdot10^{18}$ cm^{-3}	1.1-1.6eV

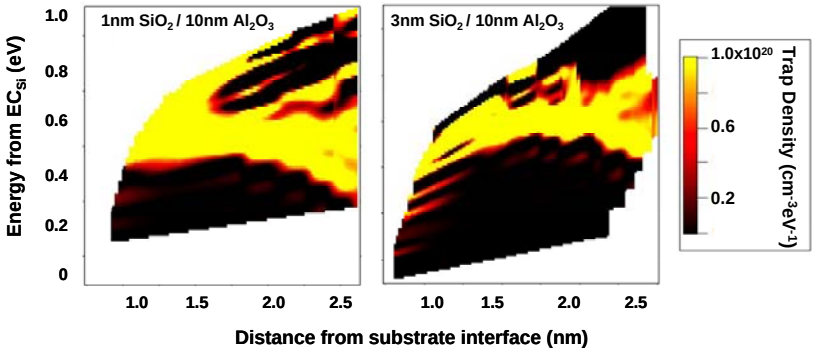

Fig. 4. Spatial-energy trap map obtained from TSCIS: thicker SiO_2 exhibit similar trap properties as thinner SiO_2, suggesting a severe intermixing.

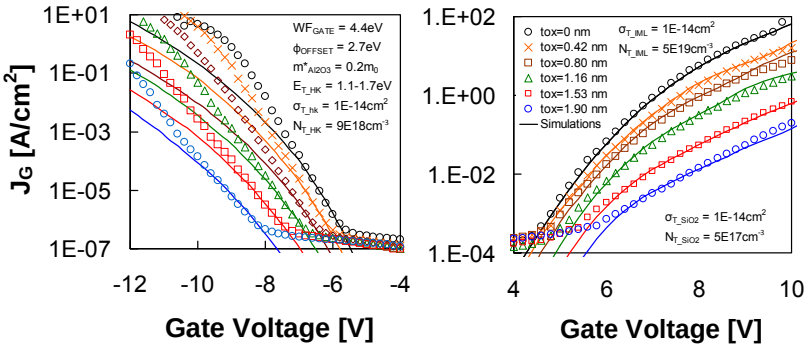

Fig. 6. Measured (symbols) and simulated (solid lines) Ig-Vg for $V_G<0$ (left plot) and $V_G>0$ (right plot) across SiO_2/Al_2O_3 stack. Simulation inputs are stack parameters (thicknesses and offset as defined as in fig. 5) and the trap parameters (density, cross section, energy levels, see Table I).

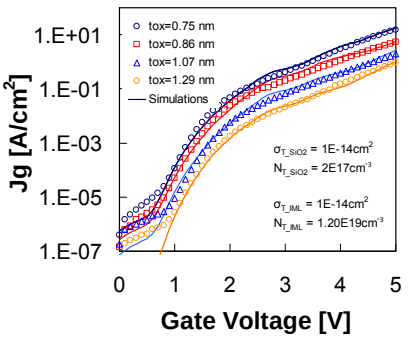

Fig. 8. Measured (symbols) and simulated (solid lines) Ig-Vg for $V_G>0$ across HfSiO stack. Simulation inputs are stack parameters (thicknesses and offset as defined as in fig. 7) and the trap parameters (density, cross section, energy levels, see Table II).

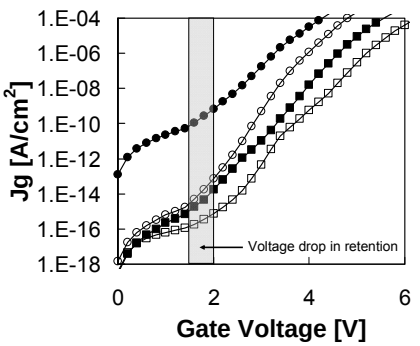

Fig. 9. Leakage current simulations across SiO_2/Al_2O_3 stack for thinner (slant tox=1 nm, 'O' symbol) and thicker (slant tox=1 nm, '□' symbol) slanted SiO_2. Filled (empty) symbols indicates simulation results with (without) taking into account the IML. The shaded area represents the typical voltage drops in data retention conditions.