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Comprehensive Modeling of Threshold Voltage Variability Induced by Plasma Damage in Advanced MOSFETs

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1. Introduction

With the scaling of advanced MOSFETs, the variation of device parameters such as "V_{th}-variability" has been recently focused [1]. This issue is primarily discussed from the viewpoint of the gate line-edge roughness (LER) [2] or the fluctuation of impurity doping. Plasma processing is widely used in manufacturing process and plasma-induced damage (PID) has been studied extensively. In general, PID is classified as charging damage, physical damage and radiation damage [3]. The charging damage induces the gate dielectric reliability degradation [3], while the physical damage, Si recess structure, leading to device performance change [4][5]. However, there have been few reports on the effects of PID on V_{th}-variability which will be extremely significant for realizing high performance devices. In this article, the effects of the charging and physical damage on the device performance degradation are comprehensively modeled in terms of the plasma-induced V_{th}-variability.

2. Model for plasma-induced threshold voltage shift

Basic mechanisms of PID are illustrated in Fig. 1. Both charging and physical damage are focused in the below.

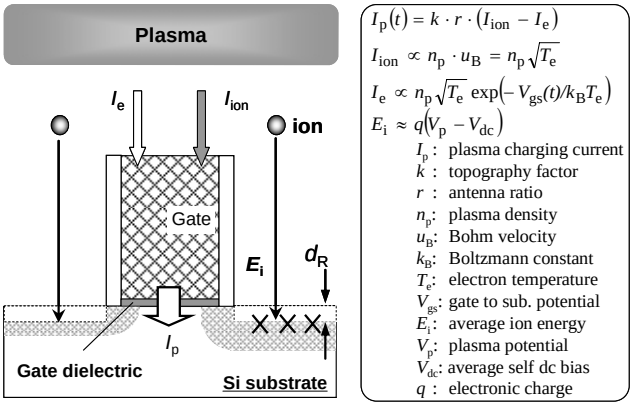

Fig. 1 Mechanisms of PID and the basic equations.

Threshold Voltage Shift Variation by Charging Damage

Charging damage is attributed to conduction current from plasma as shown in Fig. 1. (Note that plasma is considered to be a current source.) This charging current induces performance degradation, i.e., threshold voltage shift (ΔV_{th}). For reliability assessment, the electrical stress-induced ΔV_{th} such as bias temperature instability (BTI) has been extensively studied, and its field dependence has been reported [6]. As discussed later (Fig. 2), the dependence of ΔV_{th} on the stress current density I_{stress} can be described by,

$$\Delta V_{th} \cong g(T) \cdot t_s{}^n \cdot I_{stress}{}^\alpha \Rightarrow I_p{}^\alpha \ (\sim r^\alpha), \quad (1)$$

where $g(T)$ and t_s are the temperature-acceleration factor and stress time, respectively. n and α are the respective power-law components. From Fig. 1 and eq. (1), one can obtain for the charging-induced ΔV_{th}-variability,

$$\left|\delta(\Delta V_{th})/\Delta V_{th}\right|_{Charging} \approx \alpha \left|\delta(I_p)/I_p\right|. \quad (2)$$

Thus, the ΔV_{th}-variability depends on variations of the plasma and device parameters as suggested in Fig. 1.

Threshold Voltage Shift Variation by Physical Damage

Si recess structure is associated with the physical damage and has become a key issue [4]. The recess depth (d_R) depends on the energy of ion from plasma and the surface reaction layer thickness [5]. As shown later (Fig. 4), we can write its dependence on plasma parameters as,

$$d_R = A \cdot (V_p - V_{dc})^\beta = A \cdot E_i{}^\beta, \quad (3)$$

where A is a constant and β is the power-law component dependent on process conditions. The dependence of ΔV_{th} on d_R was found to be expressed by [7]

$$\Delta V_{th} \approx -B \cdot d_R / L_g, \quad (4)$$

where B is defined by device structural parameters [7] and L_g is the gate length. Thus, one can obtain

$$\left|\delta(\Delta V_{th})/\Delta V_{th}\right|_{Recess} \approx \left|\delta(d_R)/d_R\right| \approx \beta\left|\delta(E_i)/E_i\right|. \quad (5)$$

Note that the range of ΔV_{th} variation ($\left|\delta(\Delta V_{th})/\Delta V_{th}\right|\Delta V_{th}$) should also be considered for evaluating the V_{th}-variability.

3. Experimental

The damage was produced in an inductively coupled plasma (ICP) reactor with an Ar gas for 30 s. RF bias at 13.56 MHz was applied with various powers ranging from 0 to 150 W. Plasma diagnostics determined the average self dc bias (V_{dc}) and the plasma potential (V_p). The present configuration results in an average impacting ion energy E_i (= $q(V_p - V_{dc})$) ranging from 11 to 190 eV. N-MOSFETs with 7-nm-thick SiO_2 and high-k gate stack ($HfAlO_x/SiO_2$) were used for the charging damage study. Drain current-voltage (I_d-V_g) characteristic were obtained for various devices (different antenna ratios). N-type Si wafers were used for the physical damage study and the I_d-V_g characteristics were simulated by TCAD with various d_R being introduced, by assuming an offset spacer etch.

4. Results and Discussion

Figure 2 shows typical examples of I_d-V_g characteristic. V_{th} is clearly shifted. By using constant current stress (CCS) and comparing the V_{th} of damaged devices (See Fig. 2), we predicted I_p as ~ 1×10^{-9} (A). This value is consistent with that determined from plasma diagnostics (3×10^{-9} (A)). As seen in Fig. 3, the ΔV_{th} increases with an increase in effective antenna ratio r. The power-law component α of r in eq. (1) was estimated to be 0.30 for the charging damage. This is consistent with the value by CCS (0.34), verifying the model by eq. (1). Therefore, we can speculate that the variations of I_{ion}, I_e, and n_p impact on the ΔV_{th}-variability by a factor of 0.30 via I_p (See Fig. 1). Moreover, one should consider two critical scenarios: (1) Although high-k devices determine similar α (0.37), they naturally exhibit larger charge trapping [3] (~ ΔV_{th}). This unique feature may enhance the V_{th} variation range. (2) Even if the variations of I_{ion}, I_e, and n_p are suppressed, that of r is difficult to be done. Consideration of the effect of antenna ratio range (a few orders) on the ΔV_{th} variation is indispensable.

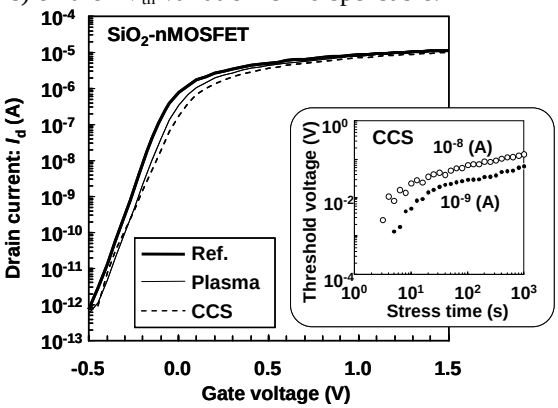

Fig. 2 I_d-V_g characteristics of plasma-exposed and constant current-stressed (CCS) samples. (W/L=30/30μm) The time dependences of V_{th} under CCS are shown in the inset.

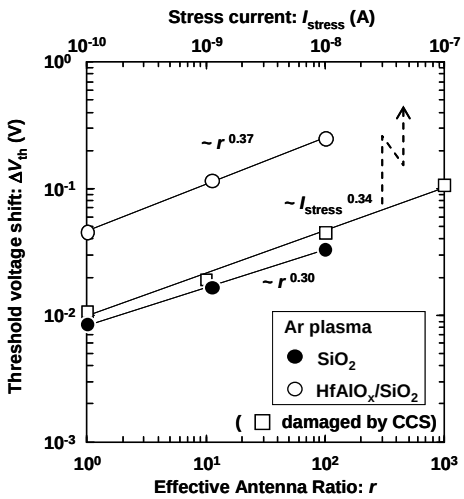

Fig. 3 ΔV_{th} as a function of antenna ratio for plasma-exposed MOSFETs with SiO_2 and high-k gate dielectrics. ΔV_{th} electrically damaged by CCS is also shown for various currents (open square).

Figure 4 shows the d_R as a function of (V_p–V_{dc}). The d_R was calculated from the thicknesses of damaged layers obtained by spectroscopic ellipsometry with optimized optical structure and from surface sputtering mechanism predicted by molecular dynamics simulations [5]. The β in eq. (3), i.e., "the impact factor" β in eq. (5), was determined experimentally to be 0.33. The ΔV_{th} calculated from TCAD for various d_R is illustrated in Fig. 5. As seen in Fig. 5, although the impact factor β is close to those by charging damage (α), one should note that the L_g shrinkage enhances the V_{th} variation range in scaled devices.

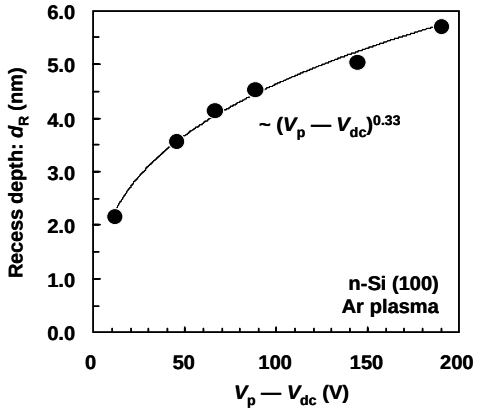

Fig. 4 Calculated recess depth as a function of (V_p–V_{dc}).

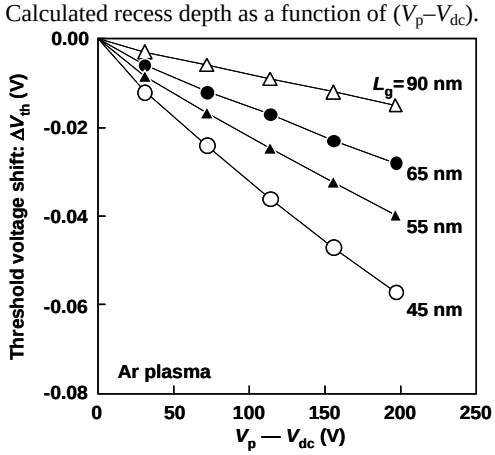

Fig. 5 Recess structure-induced ΔV_{th} as a function of (V_p–V_{dc}), estimated by TCAD for various gate length (L_g).

5. Conclusion

The impacts of plasma-induced damage on the V_{th}-variability were modeled and experimentally clarified in terms of plasma parameters. We found the similar effects on V_{th}-variability for both charging and physical damage. In addition to the above effects, one should consider that high-k dielectrics, antenna design rule and device shrinkage enhance the V_{th} variation range in advanced MOSFETs.

Acknowledgements

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