

# Characterization and Improvement of Charge Trapping in Gadolinium Incorporated Hf-based high-k/Metal gated n-MOSFETs

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## 1. Introduction:

Hf-based dielectrics are considered as the leading high- $\kappa$  candidates with metal electrode. [1] However for CMOS process implementation, carrier mobility degradation at low EOT and charge trapping-induced threshold voltage instability must be considered. [2] An interfacial oxides were used to suppress transient charging effect [3] for carrier mobility improvement, but need to compromises EOT scaling. [4] Recently, higher channel electron mobility was obtained using nitrogen incorporation to suppress gate leakage [5] and charge trap [6] due to the electron charge traps can be reduced by nitrogen atom. [7] However, it is insufficient to meet requirement at the atomic level for production. Recently, a Gadolinium (Gd) incorporated Hf-based was proposed to reduce gate leakage at low EOT. [8] However, a hysteretic effect caused by interface traps and Gd diffusion can not be understood. In this work, analysis the characteristic and reliability of Hf-based high-k/Metal gate n-MOSFETs. A post NH<sub>3</sub> nitridation was proposed to suppress the charging trapping caused by Gd diffusion through Hf oxide layer.

## 2. Experiments

A 90-nm technology was used as a vehicle to demonstrate device performances of TaC/Gd/Hf-oxide gate n-MOSFETs. Schematic illustration of this device structure is shown in Fig. 1 Following the Hf-silicate deposition with SiO<sub>2</sub> interfacial layers (a), a Gd layer was deposited with a post NH<sub>3</sub> nitridation or not (b). After the gate stack formation with a TaC metal electrode, standard backend integration was employed.

## 3. Results and Discussions

Compared with Gd/HfSiO n-MOSFETs and post NH<sub>3</sub> nitridation find the NH<sub>3</sub> nitridation offers better driving capability, smaller subthreshold swing, good Gd diffusion suppression, and less gate leakage. [9] Compared with Gd/HfO<sub>2</sub> n-MOSFETs, thinner effective dielectric thickness identified by C-V inspection was found in Gd/HfSiO gate device, as shown in Fig. 2 We found that  $V_{FB}$  shift apparently in Gd/HfO<sub>2</sub> structure due presumably to Gd diffusion through HfO<sub>2</sub> to substrate, and Gd can be suppressed by HfSiO with post NH<sub>3</sub> nitridation. In Fig. 3 shows that device instability checked by hysteresis

inspection can be improved with post nitridation especially for Gd/HfSiO n-MOSFETs.

Compared with Gd/HfO<sub>2</sub> gate n-MOSFETs, lower Nit extracted by charge pumping measurement (Fig. 4) and low frequency spectrum analysis (Fig. 5) are found in Gd/HfSiO n-MOSFETs especially with post NH<sub>3</sub> nitridation. Thus, it is presumably that Gd dopant diffusion through high-k material into Si substrate can be suppressed more efficiently with nitrogen atoms. In order to understand the impact of these interface traps on device reliability, PBI and HCI are used to inspect the process induced device degradation. We found that higher PBI induced  $I_D$  degradation (Fig. 6) and higher  $V_{TH}$  shift (Fig. 7) happened especially in Gd/HfO<sub>2</sub> n-MOSFETs. There is no apparent different in Gd/HfSiO gate n-MOSFETs with post nitridation or not, but slight larger  $V_{TH}$  shift happened on nitride Gd/HfSiO gate n-MOSFETs, which due presumably to nitrogen diffusion into substrate increase the probability of interface trapping. However, in comparison with Gd/HfO<sub>2</sub> gate n-MOSFETs, less hot carrier induced  $I_D$  degradation (Fig. 8) and  $V_{TH}$  shift (Fig. 9) happened on Gd/HfSiO gate device and slight larger device degradation happened on nitride Gd/HfSiO gate n-MOSFETs.

## 4. Conclusions

Characterization and reliability inspection for Gadolinium incorporated Hf-based gate n-MOSFETs are shown in this work. A post NH<sub>3</sub> nitridation was used to suppress Gd diffusion through Hf oxide into substrate causing interface trapping. Apparently those nitrides Gd/HfSiO gate n-MOSFETs possess better driving capability and less hysteresis happened. However, Nitrogen incorporation must be controlled carefully to avoid PBI induced and HCI induced device degradation.

## References

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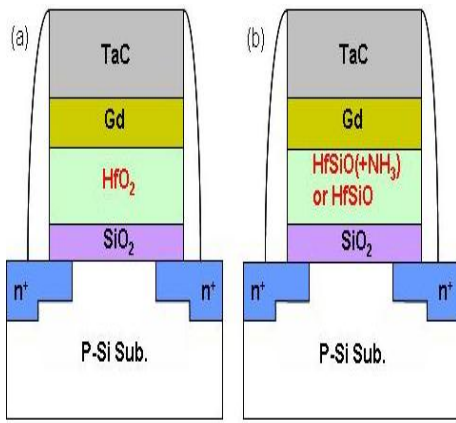


Fig.1. Process flow of n-MOSFETs with TaC/Gd/Hf-oxide gate structure.

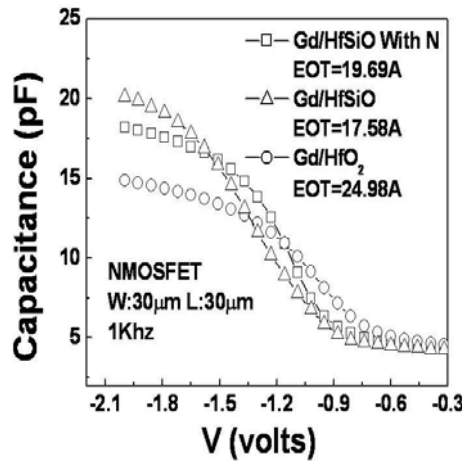


Fig.2. Thinner EOT extracted by C-V curves was found for n-MOSFETs with Gd/HfSiO gate, lower  $V_{FB}$  shift happen on nitridated Gd/HfSiO gate device.

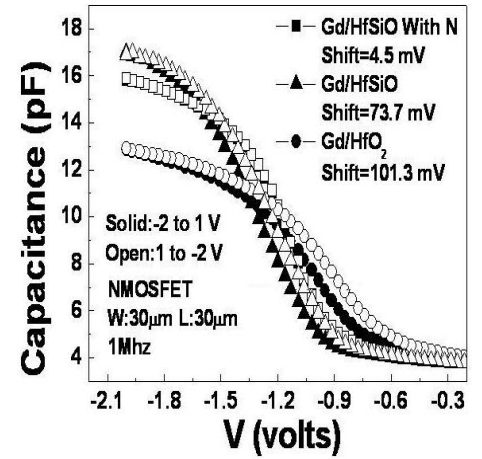


Fig.3. Less hysteresis happened on n-MOSFETs with post  $NH_3$  nitridation which can suppress interface charge trapping.

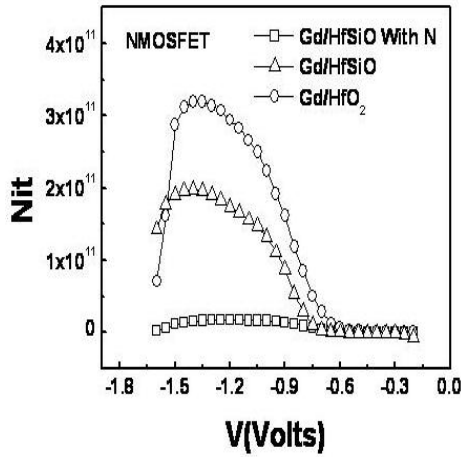


Fig.4. Lower interface defect extracted by charge pumping measurement was found for Gd/HfSiO gate n-MOSFETs with  $NH_3$  nitridation.

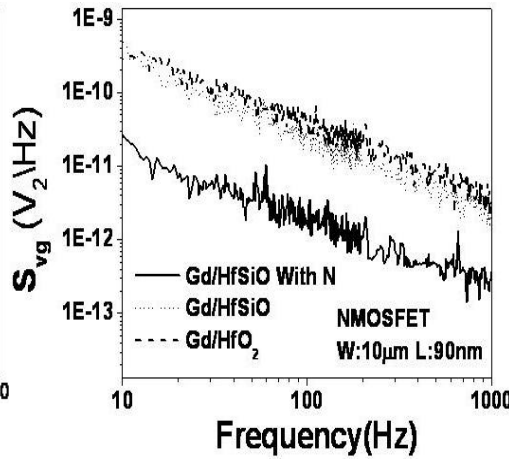


Fig.5. Lower flicker noise indicates less interface traps was found on Gd/HfSiO gate n-MOSFETs with  $NH_3$  nitridation.

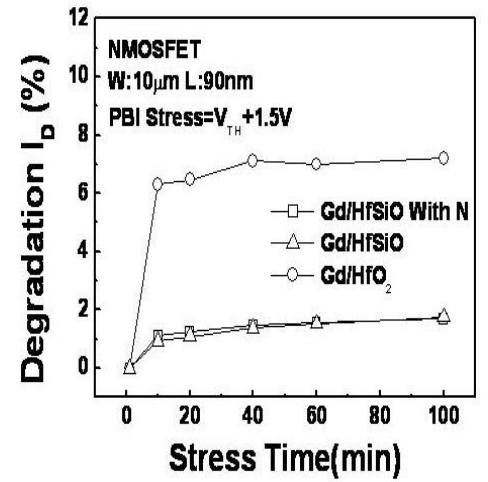


Fig.6. Less PBI induced  $I_D$  degradation was found on n-MOSFETs with Gd/HfSiO gate.

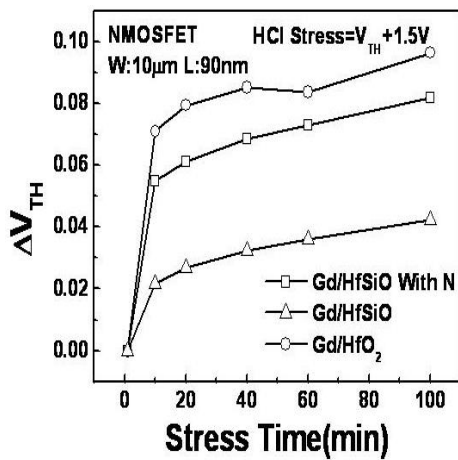


Fig.7. Less PBI induced  $V_{TH}$  shift was found on n-MOSFETs with Gd/HfSiO gate, and  $V_{TH}$  shift increased after nitridation.

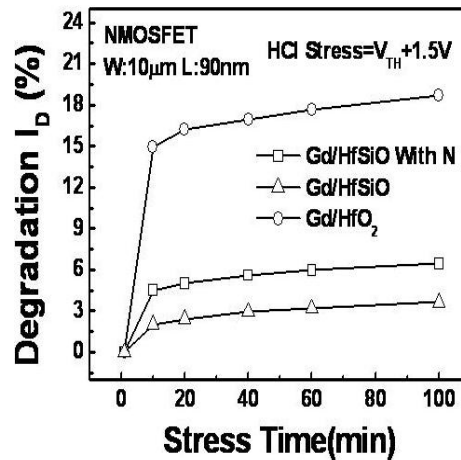


Fig.8. For HCl stress, less  $I_D$  degradation was found on n-MOSFETs with Gd/HfSiO gate. N atom caused by nitridation will increase the impact ionization rate.

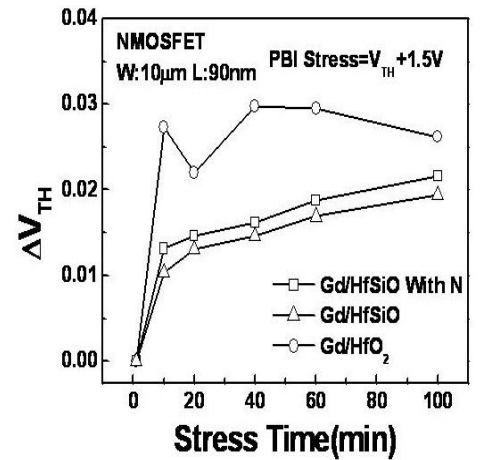


Fig.9. Less hot carrier induced  $V_{TH}$  shift was found on n-MOSFETs with Gd/HfSiO gate. Post nitridation will increase impact ionization rate.