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Threshold Voltage (V_{th}) Tunability of pMOSFETs with Ternary $Hf_xMo_yN_z$ Metal Gate and Gd_2O_3 High-k Gate Dielectric

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1. Introduction

Metal gate and high-k gate dielectric are considered to instead of poly-silicon gate and silicon oxide for 45nm generation [1]. Metal gate has advantages of low gate resistance, eliminate poly depletion effect, and boron penetration issue.

In this work, the pMOSFET device with ternary $Hf_xMo_yN_z$ metal gate and Gd_2O_3 high-k gate dielectric has been demonstrated for the first time. Threshold voltage(V_{th}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device can be tuned from -0.6 V to -0.08 V by controlling N_2 flow ratio. A physical model has been proposed to explain extrinsic Fermi-level pinning at the $Hf_xMo_yN_z/Gd_2O_3$ interface.

2. Experimental

The $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET devices were fabricated on a 4-in. n-type Si(100) using conventional self-aligned MOSFET process. After RCA cleaning, SiO_2 with thickness of 600nm as a field oxide was thermally grown by the furnace. The definition of active area and RCA cleaning were employed followed by rf-sputter of Gd_2O_3 as a gate dielectric with 6nm thickness. The $Hf_xMo_yN_z$ metal gate electrode with different N_2 flow ratio(0, 6,and 10%) were deposited by co-sputtering with pure hafnium(Hf) and molybdenum(Mo) targets in argon(Ar) and nitrogen(N_2) mixtures. The sputtering dc power of both target is 250 W. The reactive pressure and the gas flow rate are 2×10^{-3} torr and 50 sccm, respectively. The detail metal gate and high-k process conditions were shown in Table 1. The $Hf_xMo_yN_z$ gate electrodes were patterned by chemical wet etching to prevent dry etching damage. After gate patterning, S/D regions were formed by B^{11+} implantation with a dose of 3×15 cm^{-2} at 10 keV. Then, activation annealing was performed in N_2 ambient at 850°C for 30 sec. All of the samples were finally subjected to backside Al contact and sintering. The device key process flow was shown in Fig. 1. The $Hf_xMo_yN_z$ thin film with thickness of 100nm was prepared also for the thermal stability study. The basic electrical properties were analysis by a Keithley 4200 semiconductor characterization analyzer.

3. Result and Discussion

Materials and Electrical properies Characterization

$Hf_xMo_yN_z$ thin films were deposited with N_2 flow ratio of 0, 6, and 10% for resistivity study as shown in Fig. 2. The resistivity of $Hf_xMo_yN_z$ increased from 2.64×10^{-4} to 5.03×10^{-3} Ω-cm for samples without annealing as increasing N_2 flow ratio from 0 to 10%, respectively. After 950°C annealing, the resistivity of $Hf_xMo_yN_z$ thin films were below 10^{-3} order for all samples. It results in the possible application for metal gate electrode [2]. Moreover, the resistivity of $Hf_xMo_yN_z$ tended to decreased with increasing N_2 flow ratio after annealing. It may be due to $Hf_xMo_yN_z$ film phase change and is discussed with X-ray diffraction(XRD) later. In order to evaluate the N_2 and temperature effects on the phase variation, crystal orientation for the samples with N_2 flow ratio of 0, 6, and 10% were analyzed by XRD. Figure 3 shows the N_2 flow ratio effects on the crystal orientation of without and with annealing samples. From Fig. 3(a), 0% N_2 flow ratio sample only Hf(102) phase was observed. The phases of $HfMo_2$(220) and MoN(200) were shown above 6% N_2 flow ratio. Compare to the annealing samples as shown in Fig. 3(b), the phase of the $Hf_xMo_yN_z$ thin film with N_2 flow ratio more than 6% changed form $HfMo_2$(220) and MoN(200) to Mo_2N(200). It suggests that the $Hf_xMo_yN_z$ thin films were re-crystallization after high temperature annealing. Shen *et al.*,[3] has been reported the low resistivity was due to the re-crystallization of the Mo_2N structure. It is consistent with the results as shown in the Fig. 2.

The $Hf_xMo_yN_z$ metal gate electrode with Gd_2O_3 gate dielectric of pMOSFET device has been demonstrated. Figure 4. shows the typical transfer characteristic(I_{ds}-V_{gs}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET before and after native bias temperature(NBT) stress. The NBT stress conditions of stress electric field, stress time, and stress temperature are -3 MV/cm, 3200 sec, and 75°C, respectively. Before NBT stress, the parameters of threshold voltage(V_{th}) and subthreshold swing(SS) are -0.2 V and 77 mV/dec. From the Fig. 4, there is no negative bias temperature instability(NBTI) effect after NBT stress. The output characteristic(I_{ds}-V_{ds}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with 6% N_2 flow ratio also demonstrated no NBTI effect, as shown in Fig. 5.

Nitrogen Effect on Threshold Voltage Modulation

The $Hf_xMo_yN_z/Gd_2O_3$ capacitor with N_2 flow ratio of 0, 6, and 10% has been fabricated for work function modulation study. The effects of N_2 flow ratio on the C-V characteristics were shown in Fig. 6. A high N_2 flow ratio induces positive direction shift in the flat-band voltage(V_{fb}). The V_{fb} shift of about 0.6 V was obtained from 0 to 10% N_2 flow ratio. It suggested that the metal work function can be modulated by controlling N_2 flow ratio. The metal work function can be affected by stress, defects, crystalline orientation, and so on. From pervious work [4], we believe that the mechanism of the modulation in work function was speculated by crystalline orientation. The $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device with N_2 flow ratio of 0, 6, and 10% has been demonstrated. Figure 7 shows the typical transfer characteristic(I_{ds}-V_{gs}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with N_2 flow ratio of 0, 6, and 10%. The threshold voltage(V_{th}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device can be modulated from -0.6 to -0.08 V with increasing N_2 flow ratio from 0 to 10%. The V_{th} shift of about 0.6 V with N_2 flow ratio between 0 and 10%. The results were consistent with $Hf_xMo_yN_z/Gd_2O_3$ capacitors as shown in Fig. 6. Figure 8 shows the V_{th} distribution of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device. Compare to the $Hf_xMo_yN_z/SiO_2$ pMOSFET device(not show), the $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device has small V_{th} shift between 6 and 10% N_2 flow ratio. It suggested that the Fermi-level pinning effect occurs at the $Hf_xMo_yN_z/Gd_2O_3$ interface. For the V_{th} shift difference between $Hf_xMo_yN_z/SiO_2$ and $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET devices, we proposed a physical model to explain Fermi-level pinning effect, as show in Fig. 9. The $Hf_xMo_yN_z/SiO_2$ structure has little interface states (Fig. 9(a)), however the effective extrinsic interface states occurs near the valence band for $Hf_xMo_yN_z/Gd_2O_3$ structure (Fig. 9(b)) and creates a dipole that tends to drive the band lineup toward the valence band position.

4. Conclusion

The $Hf_xMo_yN_z$ thin film has excellent thermal stability up to 950°C. The $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device with N_2 flow ratio of 0, 6, and 10% has been demonstrated. The V_{th} of the $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device can be modulated from -0.6 V to -0.08 V by controlling N_2 flow ratio. This is due to the crystal orientation effects on the work function. Moreover, there is no NBTI degradation of the $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device. A physical model has been proposed to explain that the extrinsic Fermi-level pinning at the $Hf_xMo_yN_z/Gd_2O_3$ interface. Ternary Hf-Mo-N thin film is a promise metal gate for the future application.

Acknowledgment

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Reference

[1] IRTS, Semiconductor Industry association, San Jose, CA, 2007.
[2] H. Y. Yu et al., IEEE Trans. Electron Devices, 51, 609, 2004.
[3] Y. G. Shen et al., Sci. Eng., B, 95, 222, 2002.
[4] C. S. Lai et al., Jpn. J. Appl. Phys, 47, 2442, 2008.

Table 1

Process Condition	
Gd_2O_3	Pressure: 10mtorr RF power:100 W Ar/O_2:21:3(sccm)
$Hf_xMo_yN_z$	Pressure:2 mtorr DC power:250 W N_2/(Ar+N_2):0,6,10%

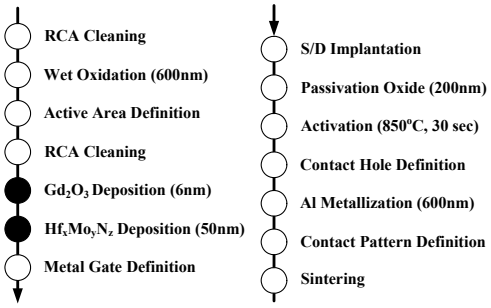

Table 1 show the metal gate and high-k process condition. Fig. 1 The conventional self-aligned process flow of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET device.

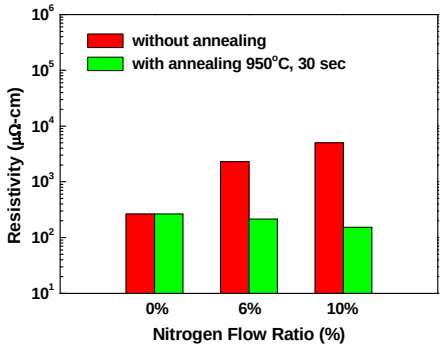

Fig. 2 Influence of N_2 flow ratio on the resistivity of the $Hf_xMo_yN_z$ thin films deposited on the silicon oxide. After annealing, the resistivity of $Hf_xMo_yN_z$ thin film was low that without annealing due to re-crystallization.

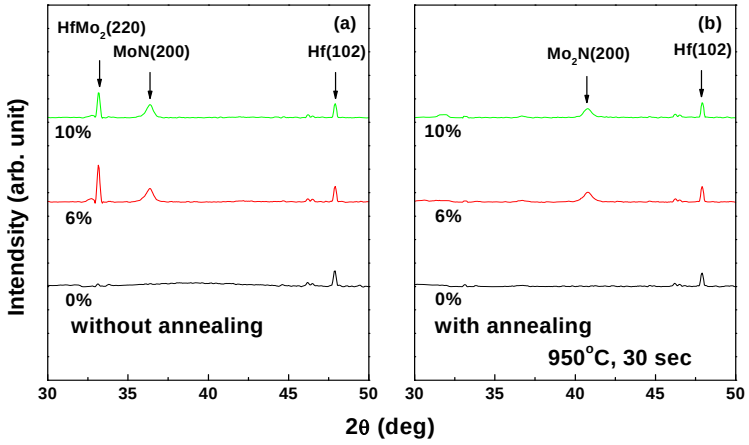

Fig. 3 The XRD patterns of $Hf_xMo_yN_z$ thin films with different N_2 flow ratio. (a)without annealing and (b)with annealing 950°C for 30sec. Without annealing sample, only shows the phases of $HfMo_2$(220), MoN(200), and Hf(102). After annealing, the phases change from $HfMo_2$(220) and MoN(200) to Mo_2N(200).

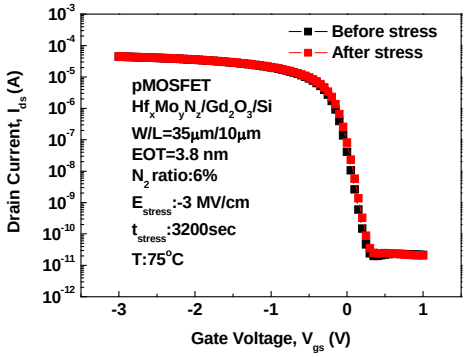

Fig. 4 The typical transfer characteristics (I_{ds}-V_{gs}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with 10% N_2 flow ratio. Before stress the parameters of threshold voltage(V_{th}) and subthreshold swing(SS) are -0.2 V and 77mV/dec, respectively.

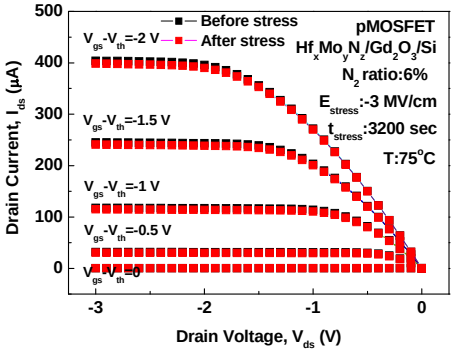

Fig. 5 The output characteristics(I_{ds}-V_{gs}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with 10% N_2 flow ratio. The stress conditions of electric field, time, and temperature are -3MV/cm, 3200 sec and 75°C, respectively.

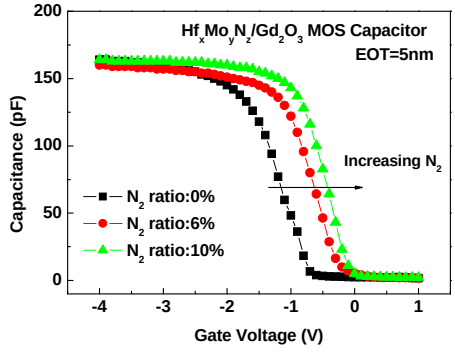

Fig. 6 The C-V curve characteristics of $Hf_xMo_yN_z/Gd_2O_3$ MOS capacitor with 0, 6, and 10% N_2 flow ratio. The flat-band voltage (V_{fb}) shifts in a positive direction with increasing N_2 flow ratio.

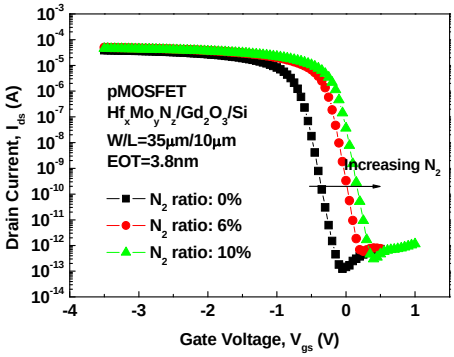

Fig. 7 The typical transfer characteristics (I_{ds}-V_{gs}) curve of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with 0, 6, and 10% N_2 flow ratio. The threshold (V_{th}) shifts in a positive direction with increasing N_2 flow ratio.

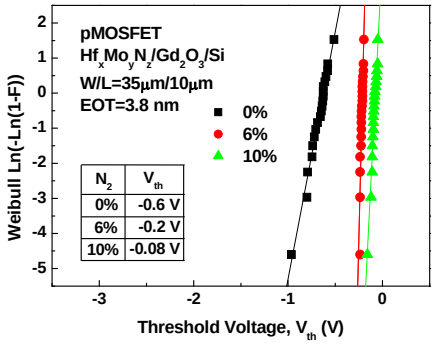

Fig. 8 Threshold voltage(V_{th}) distribution of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET with 0, 6, and 10% N_2 flow ratio. The threshold voltage(V_{th}) of $Hf_xMo_yN_z/Gd_2O_3$ pMOSFET shifts from -0.6 V to -0.08 V between N_2 ratio of 0 and 10%.

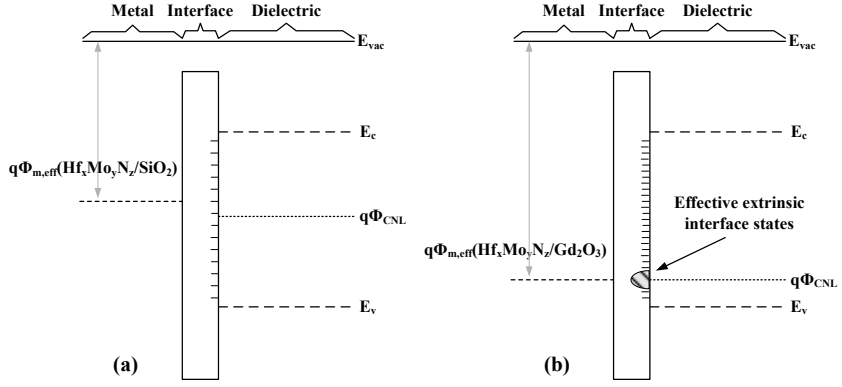

Fig. 9 Schematic energy band diagram for (a)$Hf_xMo_yN_z/SiO_2$ shows little interface states and (b)$Hf_xMo_yN_z/Gd_2O_3$ shows effective extrinsic interface states near the valence band that pin the Fermi-level.