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High Performance ZnO Thin-Film Transistors Using High-κ TiHfO Gate Dielectrics

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1. Introduction

ZnO-based TFTs have attracted much attentions duing to their good device performance, low cost, and potential to realize transparent and flexible active circuits. However, most of ZnO TFTs suffered from high threshold voltage (V_T), poor subshreshold swing (SS), and high operation voltage, setting a limit on their applications. These issues mainly result from the use of low dielectric materials (such as SiO_2) which usually leads to poor gate control on the channel current. Recently a lot of efforts are made to find suitable material for gate dielectrics of ZnO TFTs [1]-[4]. In this study, firstly, we integrated high-κ TiHfO material into ZnO TFTs for its high dielectric constant [5][6] and a promising result of low V_T of 0.34 V, small SS of 0.23 V/dec, good I_{on}/I_{off} ratio of 10^5, and high mobility of 2.1 cm^2/V-s. was attained.

2. Experiments

Figure 1 shows the process flow of the ZnO TFTs using conventional bottom-gate structure. A Si wafer with a 500-nm-thick wet oxide on it was used as the substrate. Then a 50-nm-thick TaN layer was deposited by reactive sputtering as the bottom gate electrode. It is followed by a 50 nm TiHfO film deposited by RF co-sputtering using TiO_2 and HfO_2 targets in a gas mixture ratio of O_2/Ar of 1/10 sccm/sccm[6]. The prepared samples were subjected to a post deposition annealing (PDA) in oxygen ambient at 300~600°C to evaluate the temperature influence on the high-κ defects and device characteristics. After that, a 40-nm-thick ZnO film was deposited by sputtering at room temperature. Finally, 300 nm Al was deposited by thermal coater to form the source and drain. Note that all device patterns were defined through shadow masks and Metal-insulator-metal (MIM) capacitors were also fabricated to estimate the gate capacitance and leakage current.

3. Results and Discussions

Figures 2 and 3 show the C-V and J-V characteristics of the prepared TaN/TiHfO/Al MIM capacitors. It is seen that PDA at 500°C yielded the highest capacitance and lowest leakage current. From the highest capacitance of 7 fF/μm^2 and the physical thickness of 50 nm, we estimated this TiHfO dielectric has a high κ value up to 40 which should much benefit the driving current of ZnO TFTs. However, capacitors with high-κ material annealed at 600°C reveal abnormal capacitance and leakage characteristics (not shown) because the bottom TaN gate couldn't survive in the high temperature and long time O_2 ambient. Figure 4 shows the XRD analysis of TiHfO films annealed at different temperatures. Obviously, in the range of 300~600°C, these high-κ films remain in amorphous state, which is helpful to reduce the gate leakage current. Nevertheless, the lower annealing temperature causes two orders of magnitude higher leakage current than the best condition at 500°C. This could be attributed to the unrepaired oxygen defects at low temperature treatment more than that at relative high temperatures, which is evident in the XPS analysis shown in the inset of Fig. 4. In Fig.5, we compared the I_D-V_G characteristics of ZnO TFTs with their dielectrics annealed at different temperatures in the range of 300~600°C. In the reversed bias region, the leakage current raises two orders higher of magnitude for the lower-temperature treated cases. Still, the devices with 600°C-annealed-dielectric shows failed characteristics because of the degradation of the bottom TaN gate. Figure 6 and 7 show the well-behaviored output and transfer characteristics of ZnO TFTs with the TiHfO dielectric annealed at optimum temperature of 500°C. We extracted the basic performance index of TFTs from the transfer characteristics curve shown in Fig. 7. High mobility of 2.1 cm^2/V-s had been achieved even its channel layer was fabricated at room temperature by a simple sputtering method. These devices also showed low V_T of 0.34 V, small SS of 0.23 V/dec, and good I_{on}/I_{off} ratio of 10^5. Table 1 summarizes the comparison of ZnO-based TFTs with variant unconventional dielectrics. The performance of our devices compares well with that for other devices and shows a higher mobility, smaller SS, larger I_{on}/I_{off} ratio, and comparable V_T.

4. Conclusions

High performance bottom-gate TFTs with ZnO channels with a high mobility, low V_T, small SS, and good I_{on}/I_{off} ratio have been successfully developed with high-κ TiHfO dielectrics. The mobility, V_T, SS, and I_{on}/I_{off} are 2.1 cm^2/V-s, 0.34 V, 0.23 V/dec, and 10^5, respectively.

Acknowledgements

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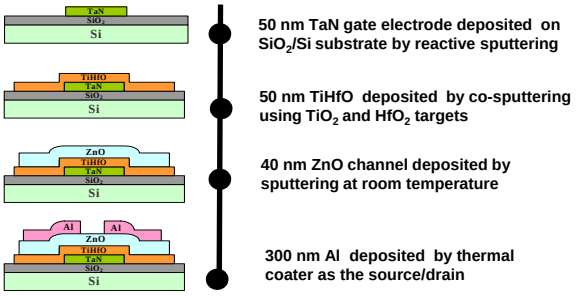

Fig. 1. Schematic cross section diagram and process flow of ZnO TFTs with the high-κ TiHfO as dielectric.

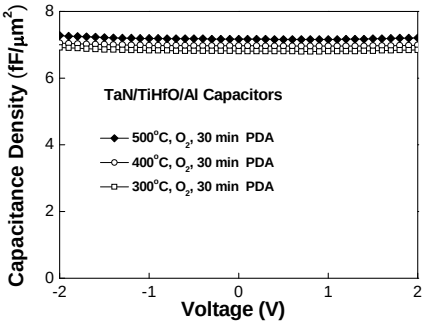

Fig. 2. MIM C-V characteristics of TaN/TiHfO/Al capacitors with the high-κ dielectric annealed at different temperatures.

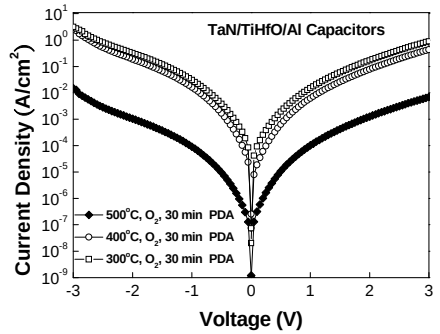

Fig. 3. Leakage current comparison of TaN/TiHfO/Al capacitors for different high-κ annealing temperatures.

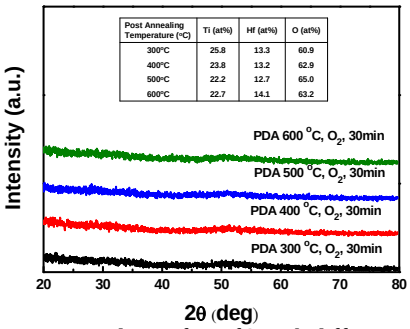

Fig. 4. XRD analysis of TiHfO with different annealing treatment. The inset shows the atomic composition ratio from XPS analysis.

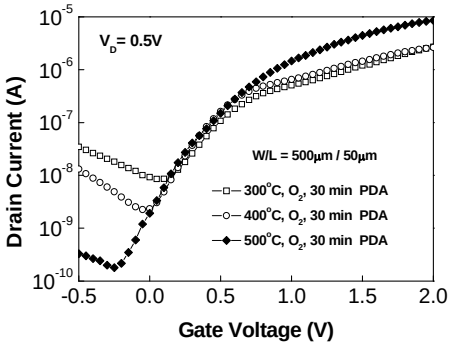

Fig.5 I_D-V_G characteristics of ZnO TFTs with the TiHfO gate dielectric annealed at different temperatures.

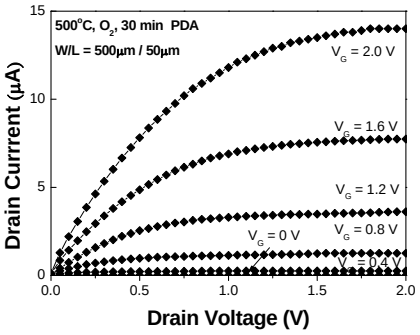

Fig. 6. I_D-V_D characteristics of ZnO TFTs with the TiHfO gate dielectric annealed at 500°C

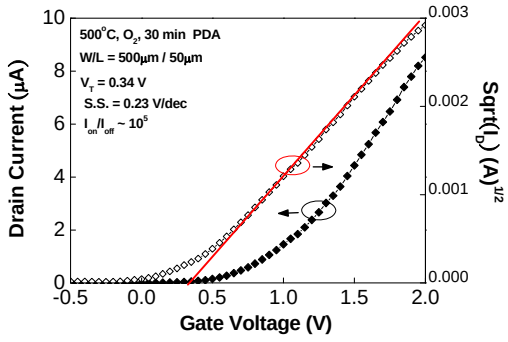

Fig7. I_D-V_G characteristics of ZnO TFTs with the TiHfO gate dielectric annealed at 500°C .

TABLE. 1. Characteristics comparison of ZnO TFTs with variant dielectrics.

Dielectric (nm)	***TiHfO (50) (This Work)***	$CeSiO_x$/ PVP(50/45)[1]	Al_2O_3 (200)[2]	P(VDF-TrFE)/ PVP(200/30)[3]	AlO_x/TiO_x/ AlO_x(22)[4]
C_i (nF/cm^2)	***700***	90	30	26	220
μ_{eff} (cm^2/V-s)	***2.1***	0.48	0.75	0.3	0.66
V_T (V)	***0.34***	0.3	1.3	-1	0.2
SS (V/dec)	***0.23***	1	1.27	2.5	0.5
I_{on}/I_{off}	***10^5***	5x10^3	1.2x10^3	10^3	5x10^3