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Device Characteristics of Short-Channel Organic Field-Effect Transistors

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1. Introduction

Organic field-effect transistors (OFETs) have attracted growing interest as a promising device to fabricate flexible, low-cost electronics such as active-matrix displays, electronic papers, and radio-frequency identification tags. To satisfy increasing demands for high speed switching, high scale integration and high output current, the downscaling of the channel lengths (*L*) of OFETs, which are typically several tens of micrometers, into the sub-micrometer regime is expected to be a critical issue. However, the short channel OFET typically suffers from a large space-charge limited current (SCLC), which is caused by the application of a high electric field along the organic semiconductor channel and significantly degrades the transistor characteristics such as a parabolic source-drain current-voltage (I_d-V_{ds}) characteristic without a current saturation and the increase in off current [1-4]. Tsukagoshi *et al.* have recently found that such short-channel effects in OFETs can be suppressed by the effective application of a gate electric field using an ultra thin gate insulator and have suggested that the presence of a high resistive region in the contact also suppresses the short-channel effects to reduce the net source-drain electric field [3,4]. It is well known that the contact resistance in OFETs causes the decrease in field-effect mobility; however an approach to suppress the short-channel effects using the contact resistance is technologically useful because it enables us to operate short-channel OFETs even by a relatively thick gate insulator, which improves the reproducibility for both device fabrication and characteristics.

In this study, we demonstrate that the short-channel effects in OFETs can be suppressed by controlling the contact resistance via the ionization potential of organic semiconductors. The bottom-contact *p*-type OFETs having *L* ranging from 5 µm down to 30 nm were fabricated using polymer semiconductors having different ionization potentials. The short-channel behaviors are remarkably reduced with increasing ionization potential of polymer semiconductors, indicating the increase in the contact resistances. The transistor operations in OFETs with 30 nm channels are achieved by using a relatively thick gate insulator.

2. Experiments

A heavily doped Si substrate with a thermally grown SiO_2 layers whose thickness was 200 nm or 50 nm was used in this study. The Au/Ti source-drain electrodes with different *L* (5 µm-30 nm) were patterned on the SiO_2 surfaces using electron beam lithography and lift-off technique. The channel width (*W*) was scaled to maintain *W/L*=10. The substrate was ultrasonically cleaned in acetone and 2-propanol, followed by UV/O_3 cleaning. Then, the SiO_2 surface was chemically modified with self-assembled monolayers (SAMs) of phenethyltrichlorosilane (PETS) or octadecyltrichlorosilane (ODTS) to enhance the field-effect mobility. Finally, the semiconductor layers were deposited on the substrate surfaces by spin coating or drop casting, followed by annealing at 100 ºC in vacuum to remove adventitious dopants such as O_2 and H_2O. For the organic semiconductors, we used three different semiconducting polymers of poly(3-hexylthiophene) (P3HT) , poly(2,5-bis(3-hexadecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT), and poly(9,9-dioctylfluorene-co-bithiophene) (F8T2), whose ionization potentials were 4.9 eV, 5.1 eV, and 5.5 eV, respectively. The *I-V* measurements of fabricated OFETs were performed in vacuum in a probe station using source meters at room temperature.

3. Results and Discussion

Figures 1(a), 1(b), and 1(c) show the output characteristics of P3HT FETs with the *L* of 1000 nm, 100 nm, and 30 nm, respectively. The SiO_2 thickness was 200 nm. The I_d-V_{ds} characteristics become parabolic and the I_d at the gate voltage V_g=0 V increases as the channel length reduces, which are consistent with the previous results in the literature [1,2]. Such behaviors have been explained by the increase in bulk current due to the SCLC. In the P3HT FETs, the source-drain Au electrodes form ohmic contact to P3HT [5], and the application of the V_{sd} to the sub-micrometer channel leads to an extremely high source-drain electric field, resulting in that the I_d is dominated by the SCLC.

Figures 2 and 3 show the output characteristics of pBTTT FETs and F8T2 FETs on 200 nm thick SiO_2 insulators with different channel lengths, respectively. It can be seen in the figures that the parabolic I_d-V_{ds} characteristics observed in the P3HT FETs are significantly suppressed

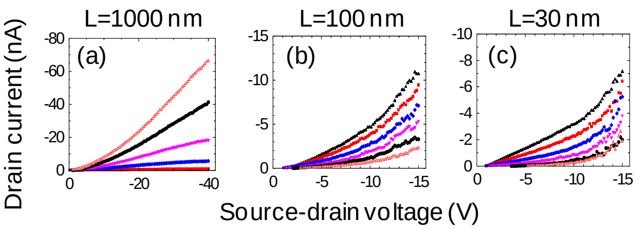

Fig. 1 Output characteristics of P3HT FETs on 200 nm thick-SiO_2 insulator with channel lengths of (a) 1000 nm, (b) 100 nm, and (c) 30 nm measured at V_g=-40 V to 10 V in 10 V steps.

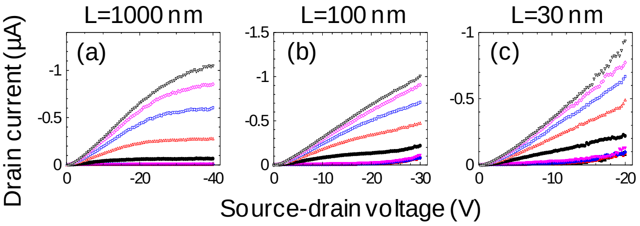

Fig. 2 Output characteristics of pBTTT FETs on 200 nm thick SiO_2 insulator with channel lengths of (a) 1000 nm, (b) 100 nm, and (c) 30 nm measured at V_g=-80 V to 0 V in 10 V steps.

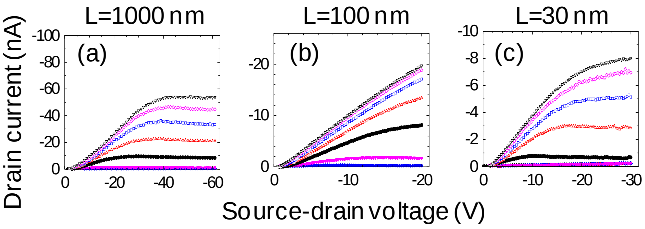

Fig. 3 Output characteristics of F8T2 FETs on 200 nm thick-SiO_2 insulator with channel lengths of (a) 1000 nm, (b) 100 nm, and (c) 30 nm measured at V_g=-80 V to 0 V in 10 V steps.

and the devices with L=1000 nm exhibit standard transistor characteristics with the I_d saturations. These results can be explained by the increase in the contact resistance due to the formation of Schottky barriers for hole injection in pBTTT and F8T2 FETs. Bürgi *et al.* have shown in scanning-probe potentiometry measurements of bottom-contact F8T2 FETs that the potential difference between the work function of source-drain Au electrodes (5.0 eV) and the ionization potential of F8T2 semiconductor (5.5 eV) clearly causes a voltage drop at the electrode/semiconductor interface, which increases the contact resistance [5]. The voltage drops at the contact would reduce the net source-drain electric field at the channel region, which suppresses the SCLC and enables to apply the gate electric field effectively [3,4]. It is also seen in the figures that the F8T2 FETs show the clear I_d saturation, while in the pBTTT FETs it becomes unclear when the channel length is below 100 nm, likely resulting from the lower ionization potential of pBTTT (5.1 eV) than F8T2 (5.5 eV). These results clearly indicate that the contact resistance and electrical characteristics of short-channel OFETs can be controlled by the ionization potential of organic semiconductors.

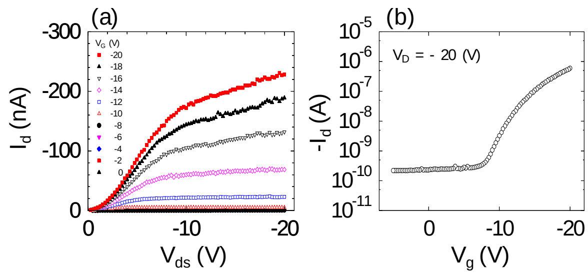

Fig. 4 (a) Output and (b) transfer characteristics of pBTTT FET on 50 nm thick SiO_2 with channel length of 30 nm.

It is expected that reducing the thickness of gate insulators leads to further suppression of short-channel effects. Figure 4 shows the electrical characteristics of the pBTTT FET on the 50 nm thick SiO_2 with the 30 nm channel. As compared with the device on the 200 nm thick SiO_2 (Fig. 2(c)), the SCLC considerably decreases and device exhibits clear saturation behaviors with a high on/off ratio of over 10^3. The average mobility was over 0.01 cm^2/Vs, which was an order of magnitude lower than that of the device with the micrometer channel. It has been expected that reducing L to nanometer regime in OFETs enhances mobility since the charge transport is limited by trapping into grain boundaries. Therefore, the optimizations of processing condition and ionization potential of organic semiconductors can lead to further improvement in the device performance of short-channel OFETs.

4. Conclusions

We have demonstrated the control of the electrical characteristics of short-channel OFETs via the ionization potential of organic semiconductors. The short-channel effects due to the SCLC are suppressed by increasing ionization potential of polymer semiconductors, which are attributed to the increase in the contact resistance. The 30 nm channel OFETs with clear saturation behaviors were successfully fabricated.

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