Interface Characterization and Charge Storage Effect of a Polystyrene Gate Dielectric Organic Thin-Film Transistor

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1. Introduction

Polymer insulators, such as PVP or polystyrene (PS) [1], have been investigated as gate dielectric layer for realization of all organic TFT (OTFT). To build an integrated circuit using organic circuits, the electrical characterization of the interface between a layer of pentacene and organic gate dielectric, such as workfunction and interface states, needs to be carried out. However, only limited studies have been reported for characterizing the interface and they have been mainly done using UPS or XPS [2], [3]. In this work, we characterize the interface of the pentacene and polystyrene gate dielectric layer by utilizing C-V measurements. Also, we present a dynamic charge storage effect of an OTFT using a direct C-V measurement on the OTFT.

2. Device Fabrication

A metal-insulator-semiconductor (MIS) capacitor and a top contact OTFTs were fabricated on a glass substrate. A 100 nm-thick Al layer was thermally evaporated under vacuum as the gate electrode. For the gate dielectric layer, a polystyrene (PS) in toluene was spin coated, followed by a curing process at 140 °C for 6 hours. By varying weight percentage of polystyrene in toluene, the thickness of the polystyrene layer was controlled. After completion of the curing processes, a 40 nm thick pentacene layer was thermally evaporated onto the sample. A top contact OTFT or a MIS capacitor was constructed by forming 40 nm-thick Au electrodes in the thermal vaporization process.

3. Measurements and Discussion

The C-V curves for all of samples reveals typical p-type behavior and exhibited a very small shift of 0.3 V in the flat band voltage (V_{FB}) as shown in Fig. 1, indicating negligible behavior and exhibited a very small shift of 0.3 V in the flat band voltage (V_{FB}) as shown in Fig. 1, indicating negligible.

where \( \phi_{ms} \) is workfunction difference between metal and pentacene, \( Q_t \) is fixed charge density, \( t_i \) is thickness of gate dielectric and \( \kappa \) is gate dielectric constant. Linear dependence of \( V_{FB} \) on thickness of the PS implies the densities of the mobile ions and trapped charge inside the PS are negligible compared to the density of the interface charges. Based on the slope of the plot, the fixed charge density can be calculated. The fixed charge density is estimated to be 2.5 \times 10^{11} \text{ cm}^{-2} which is remarkably low and comparable to one in SiO_2/Si. Also, the negative slope of the plot indicates the positive charges are likely formed at the interface of the pentacene and the polystyrene. Such a low level of the fixed charge density suggests spin-coated organic TFT may be suitable for manufacture. The extracted workfunction difference (\( \phi_{ms} \)) was found to be 0.35 eV in Fig. 3. Use of the extracted \( \phi_{ms} \) results in workfunction of \( \phi_v = 0.65 \text{ eV} \) for the pentacene when the workfunction of 4.3 eV is used for the Al electrode. The extracted value appears to be slightly large compared to previously reported values [2], [3]. We believe it may be attributed to less interface dipole induced by the low-k PS.

For direct C-V measurement on an OTFT, the gate electrode and the source/drain electrodes were patterned for minimization of fringe current and peripheral parasitic capacitance. I-V measurements were carried out with a semiconductor parameter analyzer (HP 4145B) in the dark, in ambient air with a relative humidity of ~30 % at room temperature. The measured I-V characteristics are shown in Figs. 4. For the direct C-V measurement, the source and the drain were electrically shorted, and they were connected to the low terminal (virtual ground) of the LCR meter (HP 4192A). The gate electrode was connected to the high terminal of the LCR meter while a varying dc bias was applied to the gate electrode. Measured capacitance values \( C_{GDS} \) of the pentacene TFTs are shown in Fig. 5. \( C_{GSD} \) increased for \(|V_G| > |V_{FB}| \) as a hole channel was formed between the S/D electrodes. Note that the change in \( C_{GSD} \) from depletion to accumulation mode became more evident compared to previously reported work [4], because the S/D overlap capacitance (C_{OV}) decreased significantly with the patterned gate electrode; this allowed for more accurate \( C_{OV} \) measurement. To investigate the frequency response of the intrinsic C-V behaviors, we measured channel capacitance \( C_{CH} \) for varying the frequency. By subtracting the bias-dependent \( C_{OV} \) from \( C_{GSD} \), \( C_{CH} \) was obtained, as shown in Fig. 6. At a gate voltage of -30V, holes ap-
pear to respond well to a small signal of up to 10 kHz, but at a higher frequency their responsiveness degraded due to limited lateral flow of the holes. For a smaller \( V_{\text{G}} \), the cutoff frequency decreased, indicating a lower mobility of the hole. As \( V_{\text{G}} \) increased, the cutoff frequency improved because the mobility of the hole increased by filling up the traps inside the pentacene \([5]\). Such frequency-dependent capacitance can be modeled using an R-C network, as illustrated in Fig. 6. The calculated channel capacitance based on the R-C model agrees well with the measured values.

4. Conclusion
Interface charges and effective workfunction of a polystyrene gate OTFT were extracted by characterizing C-V behavior. The electrically measured workfunction of the pentacene is 0.65 eV, which is in agreement with one obtained by other means. The interface fixed and trap charge density are found to be remarkably low, suggesting spin-coated organic TFT may be suitable for manufacture. By utilizing a direct C-V measurement, channeling capacitance of the OTFT was also obtained, providing an insight in understanding charge storage behavior of an OTFT.

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References