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Instability of Amorphous-Indium Gallium Zinc Oxide (a-IGZO) Thin Film Transistors under DC and AC Bias Stress

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1. Introduction

An amorphous or polycrystalline Si:H layer as the channel have been commonly used for conventional TFTs in flat panel display industry. However, the Si-based TFTs have drawbacks such as light sensitivity, light-induced degradation and low field effect mobility. Therefore, Si:H TFT devices reduce the efficiency of light transmittance and brightness. Besides, both amorphous and polycrystalline Si:H TFTs require relatively high process temperatures (350`C and 450`C, respectively) [1] making it difficult to fabricate these TFTs on flexible substrates.

Recently, a number of reports have described the possibility of a-IGZO TFTs competing directly with the existing Si-based TFTs structures in display applications [2-3]. ZnO-based TFTs can be fabricated on plastic substrates at low temperature and have the ability to be used to produce highly uniform and large-area displays with a low production cost. In addition, high electron mobilities (>10 cm^2/Vs) in the a-IGZO TFTs channel translate to higher switching speeds. Although from the studies on the time and temperature dependence of the instability mechanisms in a-IGZO TFTs stressed at the DC bias it presents that the charge trapping not by trap generation is dominant degradation mechanism for the electrical parameters [4-6], instability of a-IGZO TFTs under AC bias stress has been paid little attention.

In this paper, we describe the effect of AC and DC bias stress on the device characteristics of a-IGZO TFTs.

2. Experimental

For investigating the DC and AC bias instability, amorphous indium gallium zinc oxide (a-IGZO) TFTs are fabricated with the inverted staggered type (Fig. 1). MoW, SiN_X, a-IGZO and MoW are deposited as the gate electrode, dielectric, channel and S/D electrodes, respectively. More detailed fabrication process has been discussed elsewhere [6]. The TFT dimension used for this research was 100×10, 21×7 and 20×10 um^2 (W ×L). All bias stress measurements were carried out at room temperature, in air and in the dark box, and a virgin device was used for each stressing condition. And the V_T is defined as the gate voltage at which the drain current reaches 10nA×W/L in V_{DS} =10.1V.

The HP 41501B pulse generator and HP 4156C precise semiconductor parameter analyzer were used to stress the TFTs and extract the transfer characteristics after DC and AC bias stress.

3. Result and Discussion

Electrical parameters were characterized through the I_D-V_G measurement on the fabricated TFTs in Fig. 2. The virgin curve shows the n-channel characteristics with a threshold voltage of 4.1 V, a high on/off ratio > 10^8 and a subthreshold slope of 0.4 V/decade. Following the superior device characteristic, result of this paper may be reliable for the a-IGZO TFTs researches.

Previously our reported result demonstrates that the C–V results of DC bias stress as a function of frequency allow us to identify whether the dominant degradation mechanism is charge trapping or trap states generation under gate and drain bias stress. If the trap generation is dominant mechanism of device instability, after bias stress C-V curves show the dispersion and stretch out phenomenon following variable frequencies, compared with the virgin characteristic in Fig. 3 [6-7]. Also our reported result indicates that the fabricated a-IGZO TFTs recover its original characteristics after a period of relaxation at room temperature without thermal annealing treatment in Fig. 4 [6]. If defect states are generated during the stress time, some bias or thermal annealing is required to recover its initial state. Especially, thermal annealing is necessary to remove any defects created during stress time. Fig. 5 shows the time dependent V_T shift phenomenon under DC bias stress condition during the stress and relaxation period up to 40000 sec. V_T is more shifted at the beginning of the initial stress period 10000 sec than the next stress period. The V_T shift amount is nearly saturated at 7V. And The V_T shift is not accompanied by the subthreshold slope change (inserted figure in Fig. 5) in our device of the geometric size (W/L=21um/7um), which indicates that trap states are not generated.

Therefore, from the above results we can see that the dominant degradation mechanism under DC bias stress condition is the charge trapping not by trap generation.

In Fig. 7, the characteristic of threshold voltage instability of the a-IGZO TFTs for different bias frequencies and bias stress conditions is illustrated. The cumulative “On time” of DC and AC unipolar (left side) and bipolar (right side) stress conditions is the same. In this case, duty cycle of 50% and R/F time of 100 nsec of AC stress was used for all devices. Definitions of “On time”, “R/F time” and “Duty cycle” are represented by the relation in Fig. 6. Under the same bias stress condition (V_G-V_T=15V), AC unipolar stress shows less V_T shift than DC stress condition. Also, V_T shift reduces as the bias stress frequency increases. The result suggests that the AC stress results in reduced charge

trapping in the interface or dielectric layer because of shorter effective "On time" and detrapping during off period time. In AC bipolar stress condition, V_T shift is further reduced by the detrapping of trapped electron than AC unipolar condition due to the negative bias period time. Fig. 8 demonstrates that both AC unipolar (left side) and bipolar (right side) stress conditions after stress time 1000 sec don`t degrade subthreshold slope, which make only the transfer characteristic curves shift. This result indicates that the degradation of a-IGZO TFTs is primarily attributed to the negative charge trapping like the DC stress condition. In order to investigate the duty cycle and R/F time dependency on device characteristic, a same bias stress (V_G-V_T=15V) is applied, and the bias frequency is fixed as 100 kHz for all devices. V_T shift under the unipolar stress condition is further reduced as the bias duty cycle decreases or R/F time increases in Fig. 9. This result also means that the reduced degradation is caused by higher detrapping rate from the interface or dielectric layer during the longer off period time and "On time" decrease.

4. Conclusions

In summary, we have investigated the effects of variable DC and AC bias stress on a-IGZO TFTs. From the I_D-V_G and C-V curves measured before and after DC bias stress and the V_T shift curves during AC bias stress time, result of this paper demonstrates that V_T instability results from charge trapping in the interface or dielectric layer under the both DC and AC bias stress conditions.

Acknowledgements

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References

[1] Y. Sun, et. al, Adv. Mater., 19, 1897, (2007). [2] J. K. Jeong, et. al, Appl. Phys. Lett., vol. 91, pp. 113505, (2007). [3] J. S. Park, et. al, Appl. Phys. Lett., vol. 90, pp. 262106, (2007). [4] J. M. Lee, et. al, Appl. Phys. Lett., vol. 93, pp. 093504, (2008). [5] A. Suresh, et. al, Appl. Phys. Lett., vol. 92, pp. 033502, (2008). [6] K. I. Choi, et. al, Cry. Va. Con. Exh., pp. 333, (2008). [7] K. C. Moon, et. al, IEEE T.-E.D., vol. 52, no. 4, (2005).

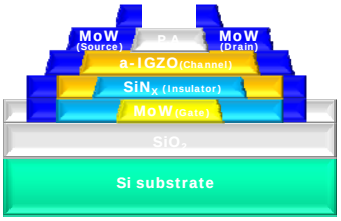

Figure 1. Schematic cross section of a-IGZO TFTs, which have an inverted staggered bottom gate structure.

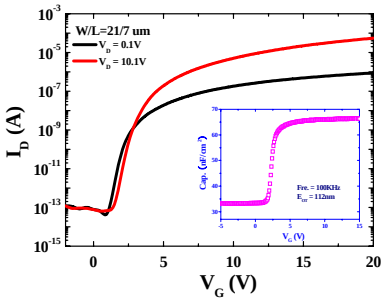

Figure 2. I_D-V_G curves of a-IGZO TFTs. Inset is Capacitance-Voltage curve indicating that E_{OT} is 112nm.

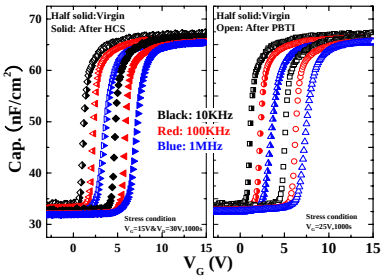

Figure 3. C–V curves at before and after stress 1000s following the variable frequencies and stress conditions [6].

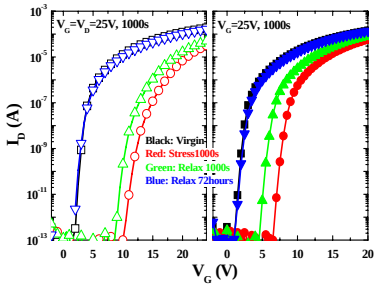

Figure 4. Transfer characteristic curves in both PBTI and HCS conditions during the stress and relaxation time at RT.

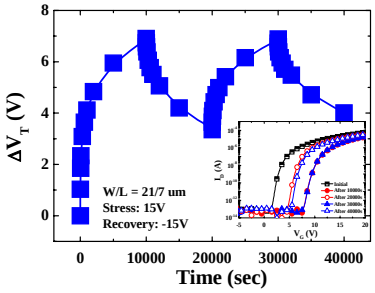

Figure 5. Time dependent V_T shift curve under the DC bias stress condition. Inserted figure is the I_D-V_G curves.

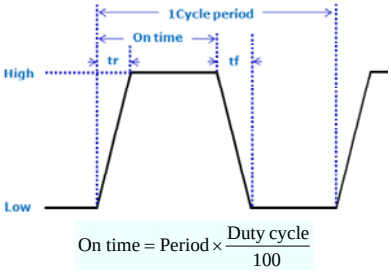

Figure 6. Definitions of "On time", "R/F time" and "Duty cycle" under the AC bias stress condition.

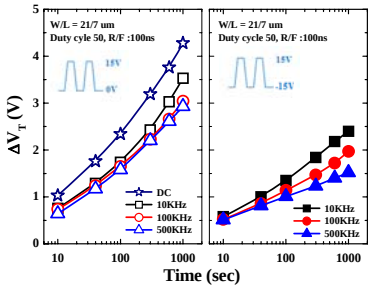

Figure 7. V_T shift curves of the a-IGZO TFTs for different bias frequencies and bias conditions. (left side unipolar and right side bipolar conditions)

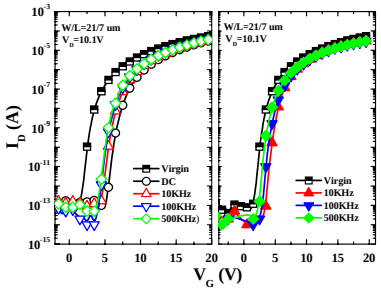

Figure 8. Both AC unipolar (left) and bipolar (right) stress conditions after stress time 1000 sec make only I_D-V_G curves shift. Subthreshold slope is not degraded.

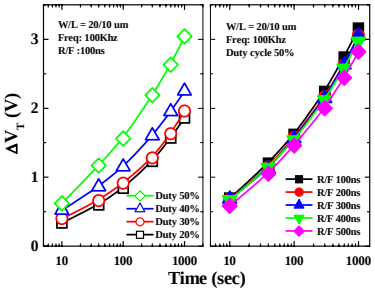

Figure 9. V_T shift is further reduced as the bias duty cycle decreases and r/f time increases under the AC unipolar stress condition.