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Interface and Passivation Effect on Subthreshold Transport of Carbon Nanotube Network Transistor by Plasma Enhanced Chemical Vapor Deposition

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1. Introduction

Thin film transistors (TFTs) of randomly networked single walled carbon nanotubes (SWNTs) have drawn recent attention as a method to provide a new type of SWNT semiconductor thin film for transparent or flexible electronic devices [1]. However, reasonably acceptable on/off ratio (~10^{-3} - 10^{-4}) was obtained at only a low tube density below the percolation threshold (~1 tube/μm^2) or a large channel length (L_c~100 μm) [2]. Difficulty to achieve the acceptable on/off ratio was attributed to the existence of metallic paths by the metallic nanotubes (M-nanotubes) with the fraction of ~33% in the random chiral distribution. The Plasma enhanced chemical vapor deposition (PECVD) could be especially useful method to build the SWNT network transistors since it fits to the standard semiconductor technique for transistor fabrication without degradation in transport by the biological and chemical treatments for the required selection process [3]. Recently, the SWNT network transistors have been successfully demonstrated with high density nanotubes grown by the PECVD above the percolation threshold [4]. In this report, effects on subthreshold transport by the types of gate dielectric and passivation are systematically presented for transistors with the random network of nanotubes which were grown by the PECVD.

2. Data and Results

SWNT networks were grown at 450 ℃ by water plasma assisted PECVD (CH_4) using a direct photolithographic technique that employed a simple mixture of ferrocene and commercially-available photoresist. 0.01M and 0.03M of ferrocene in the resist used to obtain the density (ρ) of 25 tubes and 50 tubes per μm^2 with ~0.5 μm of the nanotube length. Four different gate dielectrics were prepared as 1) 4000 Å of SiO_2 for back gate structure with ρ=25 tubes per μm^2, 2) 4000 Å of SiO_2 for back gate structure with ρ=50 tubes per μm^2, 3) 1000 Å of Al_2O_3 for back gate structure ρ=50 tubes per μm^2, and 4) 500 Å of the atomic layer deposition Al_2O_3 for top gate structure ρ=50 tubes per μm^2. Nanotube networks in the transistor channel are open for the sample 1 and 2, but passivated for the sample 3. Ti (100 nm) was used as the electrode material. Detailed fabrication method is elsewhere in literature [3].

Fig. 1 shows the transfer curves, I_{ds}-V_g for the selected channel lengths, L_c= 3 and 10 μm of two different densities. The I-V characteristics exhibit typical p-type behavior. The on/off ratio strongly depends on both of channel length and nanotube density which are correlated with percolating behavior.

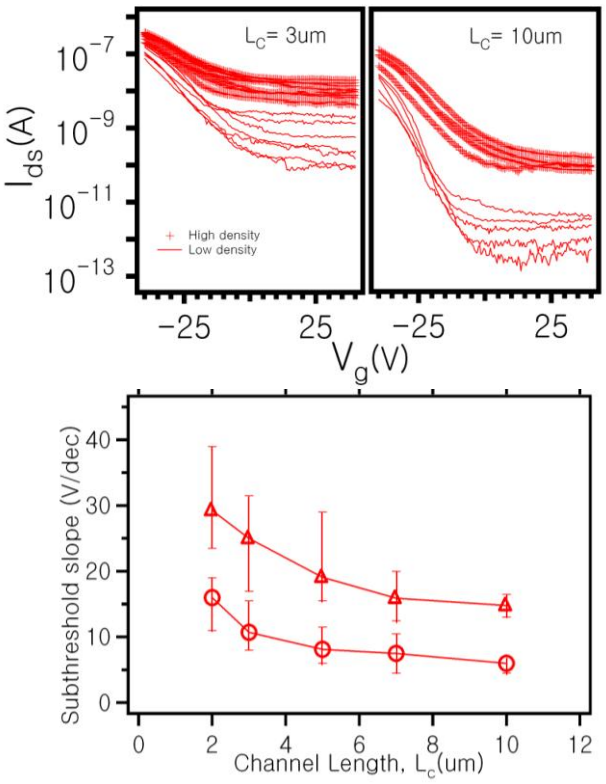

Fig. 1 The transfer curves, I_{ds}-V_g for the selected channel lengths and the subthreshold slops extracted from the transfer curves for L_c=2, 3, 5, 7, 10μm. The transfer curves, I_{ds}-V_g for, L_c= 3 and 10 μm of two different densities for 5 different transistors for each sample type: ρ=25 tubes and 50 tubes per μm^2 for low and high density. Transistors are the bottom gate structure with 4000 Å of SiO_2 for the gate dielectric. Nanotube networks in the channel are open.

Since the nanotube network is a percolating system of a mixture of the metallic (M) and the semiconducting (S) tubes, large off-current is induced by the metallic paths before the threshold. Channel length is a major factor for transport governed by the percolating behavior. Saturation

of the subthreshold slop indicates that the critical channel length is ~5μm. The on/off ratios are also saturated to the acceptable values of 10^3~10^5 above the critical channel length.

Fig. 2 shows the transfer curves, I_{ds}-V_g for the top gate structure with 500 Å of Al_2O_3 gate dielectric which also acts as a passivation layer of the nanotube channel. Insert is the back gate transistor structure with 1000 Å of Al_2O_3 gate dielectric. The channel length is 10 μm which is larger than the critical channel length. The S-slop is dramatically reduced from 10 V/decade to 0.9 V/decade with passivation.

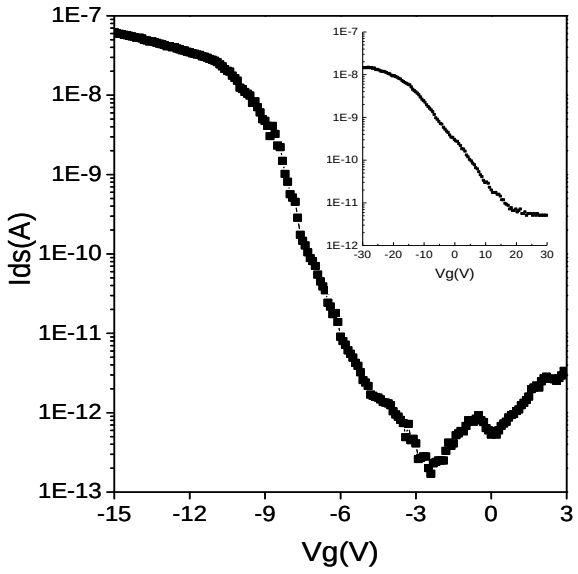

Fig. 2 The transfer curves, I_{ds}-V_g for the 10 μm channel length transistor whose nanotube density ρ= 50 tubes per μm^2. The gate dielectric is Al_2O_3 (500 Å) and acts as the passivation layer. Insert is the back gate transistor structure without passivation layer.

The subthreshold slope, $S=dV_G/d(\log I_D)$, is given by $(kT/q)\ln(10)[1+(1/C_{ox})(dQ_D/d\phi_s)]$ in the weak inversion region for the MOS devices where Q_D is total depletion charge that is evaluated for varying ϕ_s from to $2\phi_F$. From one-dimensional nature of the carbon nanotube transistors, Q_D modifies with the total trapped charges at interface between nanotubes and gate dielectric, and on nanotube surfaces. Then the subthreshold slope of the nanotube field effect transistor reduces to $(kT/q)\ln(10)[1+(C_{IT}/C_g)]$ without the quantum capacitance [5]. The capacitance, $C_{IT} = d(qN_{IT})/d(\phi_s)$, due to the total trapped hole charges (N_{IT}) is expected to be much larger than C_g, the subthreshold slop S is directly proportional to C_{IT}/C_g.

For the case of SiO_2 gate dielectric, S slops for L_c=10 μm are obtained 16 V/decade for ρ= 50/μm^2 and 8 V/decade for ρ= 25/μm^2. It leads to agreement that the trapping sites (N_{IT}) are constantly generated at interface between nanotubes and gate dielectric, and on nanotube surfaces. On the other hand, the C_{IT}/C_g of Al_2O_3 is ~0.6 C_{IT}/C_g of SiO_2 for ρ= 50/μm^2. It will be interpreted that Al_2O_3 is slightly more defective than SiO_2 if the assumption of constant inversion capacitance is used for the different interfaces of nanotubes/SiO_2 and nanotubes/Al_2O_3. It is noted that estimation of C_g is not simple and further study should be required for the accurate analysis.

Large density of nanotubes intrinsically results the poor subthreshold characteristics with increase of the total trapped hole charges (N_{IT}). The electronic device application, for example, thin film transistor with nanotube networks needs to remove the trapped charges for better transistor performance. It is required to seek a method to remove the carrier trapping centers from nanotubes. The transistor of the channel passivation actually shows more than 10 times improvement of the S-slop comparing with the channel opened transistor. It leads to about 5 times decrease of the interfacial capacitance by removing the carrier trapping centers.

3. Conclusions

In summary, we demonstrate the electrical transport for subthreshold of the carbon nanotube network transistor. The water-assisted PECVD allows a S-nanotube selective growth where the on/off ratio of the transistors is still acceptable for the nanotube density ρ= 50/μm^2 which is much higher than percolation threshold ρ= 1/μm^2. Large S-slop induced by high density networks is analyzed with the total trapped charges at interface between nanotubes and gate dielectric, and on nanotube surfaces. Gate dielectric is not a critical to generate the trapped charges by comparison with transistors of SiO_2 and Al_2O_3 as the gate dielectric. On the other hand, channel passivation results large reduction of the S-slop.

This achievement supports a method to isolate the trapping sources from nanotubes sources and suggests that the nanotube active devices may be fitted to thin film applications for the future electronics by increase the transistor performance.

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References

[1] C. Kocabas, N. Pimparkar, O. Yesilyurt, S. J. Kang, M. A. Alam and J. A. Rogers, Nano Lett. **7**(2007) 1195

[2] E. S. Snow, J. P. Novak, P. M. Campbell and D. Park, App. Phys. Lett. **82** (2003) 2145.

[3] Y. S. Min, E. J. Bae, B. S. Oh, D. Kang and W. Park, J. Am. Chem. Soc. **127** (2005) 12498.

[4] U. J. Kim[1)], E. H. Lee, J. M. Kim, Y.-S. Min, E Kim and W. Park, Nanotechnology (In press).

[5] S. Kumar, N. Pimparkar, J. Y. Murthy and M. A. Alam , App. Phys. Lett. **88** (2006) 123505.